HYBRID MULTI-LAYER CMOS-COMPATIBLE MATERIAL PLATFORM FOR HIGH-PERFORMANCE INTEGRATED NANOPHOTONICS

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HYBRID MULTI-LAYER CMOS-COMPATIBLE MATERIAL PLATFORM FOR HIGH-PERFORMANCE INTEGRATED NANOPHOTONICS

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To my parents,

Parvaneh & Mahmood

and my wife,

Maryam.

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SUMMARY

Optical interconnects are poised to replace wires in short-range communication networks at different levels including processing units in computer clusters, on-board components, processors, and even cores within a processor. With the ever-increasing need for higher data rates, there is an urgent need for new optical communication subsystems and device architectures to achieve these data rates at very low power consumption to avoid any energy dilemma. The objective of this work is to study new material platforms for integrated photonic applications, that could potentially deliver stringent system requirements for future generations of optical interconnects in terms of speed and power consumption. The different platforms that are studied here are 1) 3-D integration of Si layers; 2) using Silicon Nitride (SiN) as an alternative to Si; 3) using graphene-SiN hybrid material platform.

I used high quality wafer bonding technique to develop double-layer SOI (potentially multi-layer) material platform. To prove the performance of the platform record high quality factor devices are fabricated and tested on this platform. This enables the development of denser photonic circuits, efficient photonic-electronic integration, and high-speed, low-power modulation and tuning. I demonstrated polarization cross-coupling between quasi-orthogonal modes in double-layer SOI platform by taking advantage of unique asymmetries in etched structures. I used SiN as an alternative to Si to get around issues in Si platform such as high nonlinear coefficients, and high absorption loss at visible wavelengths. I demonstrated high-Q ultra-compact resonators in SiN platform through the combination of device engineering and using a novel etching approach with atomic-layer-

deposited-alumina as hard mask for dry etching. Tuning capability is added to the passive SiN devices through integrating graphene with SiN and demonstrating active graphene-SiN structures which could enable high-speed, low-power modulators and switches.

CHAPTER 1. INTRODUCTION

Silicon-on-insulator (SOI) is considered an excellent material platform for integrated photonic applications. Conventional integrated photonic and optoelectronic devices and systems are primarily formed on SOI substrates mainly due to its favorable optical, electrical, and mechanical properties including its relatively low loss, relatively strong thermo-optic effect (that allows for thermal tuning and reconfiguration), and relatively strong plasma dispersion effect (that enables tuning and reconfiguration by injecting free carriers) [1-4]. These features of SOI, in addition to its compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication process, have brought forth a wide range of functional devices, including high-Q resonators [5-7], electro-optic modulators [8-11], nonlinear photonic devices [12-15], and opto-mechanical devices [16-18]. SOI, however, suffers from some shortcomings that limit its application in some other important structures. Throughout the rest of this section I will address these shortcomings and introduce new material platforms and device architectures to improve them.

1.1 Double-layer Silicon-on-insulator

While SOI (i.e., a single-layer Si on SiO_2) material platform is suitable for most of photonic devices; multi-layer integrated photonic material platforms based on three-dimensional (3-D) integration of multiple Si layers enable new functionalities and more compact integration of photonic devices [19-21]. Three-dimensional integration enables the development of denser integrated photonic circuits by vertically stacking multiple layers of photonic structures on top of each other [22]. It also enables the integration of active photonic and optoelectronic devices that are constrained in the single-layer SOI

platform [22]. The availability of multi-layer Si material platform, with desired thickness in each layer and the optimal spacing between the layers, also provides a large degree of flexibility in designing photonic devices.

1.1.1 Material Platform

Several methods for fabricating 3-D, or more specifically, multilayer Si devices have been demonstrated, including separation by implantation of oxygen (SIMOX) [23, 24], hydrogenated amorphous silicon (a-Si:H) deposition [25], polycrystalline silicon (polysilicon) deposition [22, 26], and wafer bonding [20, 27]. SIMOX process requires annealing at a very high temperature (~1300º C) to cure the implantation damages [23], which limits its CMOS compatibility. On the other hand, however a-Si:H is a low-loss material [28], it suffers from much lower charge mobility compared to crystalline Si due to its amorphous nature [29], thereby limiting photonic/electronic integration [22]. Polysilicon, on the other hand, has a relatively high (~100cm^2/V-s) [30] carrier mobility. However, it suffers from high propagation loss due to scattering and absorption at the polysilicon grain boundaries [22].

Low-temperature wafer bonding is a CMOS compatible process (done at 450º C) and allows having single crystalline Si in all layers, which is essential for high performance devices that require superior optical, electrical, and mechanical characteristics. Double-layer SOI using wafer bonding with relatively thick interface oxide has been successfully used to demonstrate 3-D photonic integration [20]. However, wafer bonding with smaller interface gaps (e.g., 100 nm), which are needed for active multi-layer optoelectronic and opto-mechanical devices has turned to be challenging and previous attempts have led to

higher optical loss compared to conventional (i.e., single-layer) SOI [27]. As will be discussed in details in chapter 2, here, I used a high quality wafer-bonding technique to transfer a crystalline Si layer on top of an SOI substrate (with a thin SiO_2 interface in between) to form a high quality double-layer SOI platform. By optimizing the wafer-bonding process based on oxide-oxide covalent bonding at low temperatures (below 450°C) I was able to achieve such a platform with high optical quality. To investigate the quality of the wafer bonding and its capability for forming functional devices, I investigated the performance of compact resonators with different radii. I experimentally achieved record high Q's in multimode microring resonators with a wide range of sizes (radii in the range of 2-20 μm).

1.1.2 Polarization Cross-coupling in Double-layer SOI

Si has a relatively high refractive index (~3.47). The high index contrast between Si and SiO_2 (n~1.44) provides excellent confinement of optical modes and has enabled realization of dense, miniaturized, and low-loss structures on the SOI platform [1, 31-34]. However, this high index contrast comes at a price. For instance, it makes the devices particularly sensitive to sidewall roughness and cause optical loss through scattering [35-40]. Moreover, the high index contrast leads to sensitivity of device performance (e.g., resonance wavelength) to dimensional variations, which can be caused by random fabrication process variation or non-uniform Si thickness across the whole SOI wafer [41, 42]. Another disadvantage of the high index contrast of the SOI platform is the significant birefringence that causes polarization-sensitive characteristics for integrated photonic devices [43-47]. On the other hand, optical signals can experience random rotations upon propagating through photonic circuits [48]. Efficient polarization coupling is also critical

for devices such as wavelength-selective filters. It is therefore, necessary to come up with integrated polarization converters and splitters in which a given polarization state can be readily converted to a desired state in the photonic circuits. Different approaches have been introduced to achieve such devices. Some need multistep lithography/etching and long bulky adiabatically-tapered waveguides [49, 50]. Some other techniques are based on microrings [51]. Polarization rotators using microrings can be more compact because polarization rotation is strongly enhanced by the cavity-effect at the microring resonance frequencies. Here, I discuss and experimentally demonstrate compact cross-polarization coupling using asymmetric microrings coupled to waveguides, fabricated (in a single lithography/etching step) on the double-layer SOI platform. Previously, microrings with tilted sidewalls based on single-layer platforms were suggested as polarization rotators [52, 53]. However, the use of double-layer SOI platform [54, 55], which is used here, results in higher asymmetry in the structure and hence more efficient polarization conversion among quasi-orthogonal modes of the waveguide and the microring. As will be discussed in detail in chapter 3, the material platform (double-layer SOI) along with the fabrication process allows for fundamental TE and TM polarization modes (TE_0 and TM_0) to directly couple to each other. Coupling of TE_0 and TM_0 is usually done in two steps. First, the TM_0 is coupled to a higher order TE mode. Then, the higher order TE mode is converted to TE_0. However, in this work, the asymmetry introduced during the fabrication process makes the structure asymmetric both in the vertical and the horizontal directions which leads to direct coupling of TE_0 and TM_0. At the same time, the enhancement given by the microring cavity increases the polarization coupling efficiency; therefore, no bulky adiabatically-tapered waveguides would be needed for cross-polarization coupling. As will be discussed in

chapter 3, this is the first time cross-polarization coupling of the fundamental TM mode of a waveguide to such high radial order TE modes are demonstrated. A preliminary report of this work was presented in [56]. In chapter 3, first the theoretical background of this work is discussed then the fabrication process, experimental results, and finally the conclusion are presented.

1.2 Silicon Nitride for Photonics Applications

As mentioned earlier, SOI is an excellent material platform for photonic applications and a wide range of integrated devices have been demonstrated in this platform using Si as the device layer [5, 8, 12, 16]. Nonetheless, Si has some inherent shortcomings which limit its application for some other devices. For instance, Si suffers from significant material loss at the visible and near infrared (NIR) spectrum below 1.1 μm. Si also suffers from a relatively large third-order nonlinear coefficient [13, 57, 58] that limits the power handling capability of Si-based devices, especially resonators. In addition, the two-photon absorption in Si [15, 59-61] at high powers significantly increases the free-carrier loss and makes Si a bad choice for structures like ultra-high-Q resonators. This is while, stoichiometric silicon nitride (SiN) deposited using low pressure chemical vapor deposition (LPCVD) is proven to have considerably lower optical loss [62-64] and nonlinearity [65, 66] than Si, and has lately been used more extensively for forming structures that require low loss or large power handling capabilities (e.g., ultra-high-Q resonators) [67].

1.2.1 Ultra-compact High-Q SiN Resonators at Visible Wavelengths

Contrary to Si, SiN is transparent not only at infrared and NIR but also at visible wavelengths (from 300 nm to several microns) [68-71]. Recently, there have been several

works on ultra-high-Q resonators at visible spectrum [70, 71]. Nonetheless, a shortcoming of SiN is that it has a lower refractive index than Si (~2.0 versus ~3.47). This means that devices fabricated on SiN will have lower refractive index contrast with respect to the cladding (~0.6 with respect to SiO_2 cladding). This lower index contrast will result in higher bending loss which consequently prevents us from making ultra-compact high-Q resonators with sharp bending curves (i.e., extremely low radii). Therefore, while miniaturized high-Q Si resonators with radii as low as 1.5 μm have been demonstrated [72], there has been no report on compact high-Q microresonators with large free spectral ranges (FSR) in SiN at NIR below 1.1 μm and visible wavelengths. This puts a major limitation on the density of integrated optical circuits on SiN platform.

Here, I propose to resolve this challenge by 1) using a relatively thick LPCVD SiN film on silicon dioxide (SiO_2) substrate and 2) over-etching the microdisk resonator pattern in the bottom SiO_2 substrate. The former results in resonators with higher effective index modes, and the latter results in increasing the index contrast and distancing the resonator mode away from the leaky substrate modes and effectively reducing the bending loss. Thus, the combination of the two effects enables a higher radiation-limited Q for the resulting miniaturized SiN resonators. In chapter 4, I will first discuss the theoretical background behind this work, then the fabrication process, and experimental results are presented.

1.2.2 Graphene-SiN Hybrid Platform

Another major shortcoming of SiN is its lack of a reliable tuning mechanism. The capability to tune optical devices (e.g., resonance wavelength of resonators) is an important requirement to make reconfigurable devices such as switches, modulators. Unfortunately,

conventional tuning mechanisms that have widely been used for Si-based devices cannot be used for SiN-based ones. For instance, while reconfigurable devices based on carrier injection and depletion (through relatively strong plasma dispersion effect in Si) have been demonstrated on SOI platform [73-76], the same devices cannot be implemented in SiN due to its insulating nature. Another widely used tuning mechanism in Si is thermal reconfiguration through its relatively strong thermo-optic coefficient (TOC) [77-81]. This approach is technically possible in SiN, but because the TOC in SiN [82] is one order of magnitude lower than in Si [83], it cannot be used as an effective tuning mechanism in SiN. Moreover, thermal tuning is inherently a slow process; therefore, we need to come up with novel approaches to tune SiN-based optical devices. One example could be to integrate other materials with the SiN platform to enable efficient and fast reconfiguration techniques. One excellent candidate in doing so is graphene. Graphene is a monolayer of carbon atoms in a hexagonal lattice, and has attracted a great deal of attention due to its unique mechanical, electrical, and optical properties [84-87]. Moreover, graphene interacts remarkably with light across infrared and visible spectrum with ~2.3% absorption of normal incident light, even though it is composed of a single monolayer of atoms [88-92]. This is due to the unique zero-gap electronic band structure in graphene [93, 94]. Furthermore, the absorption spectrum of graphene can be tuned by electrostatic gating to change the Fermi level through application of voltage [95, 96]. Graphene also exhibits remarkably high carrier mobility (200000 $cm^2V^{-1}s^{-1}$) at room temperature [97, 98]. Therefore, by integrating graphene on SiN, not only tuning capability will be added to SiN-based devices, but performance of conventional Si-based integrated photonics devices could be surpassed in terms of, for example, modulation speed at much less power

consumption. In this new class of modulators based on hybrid graphene-SiN material platform, we take advantage of the high carrier mobility and the strong plasma dispersion effect of graphene combined with high light confinement in compact SiN photonic devices to enable switches and modulators with speeds that could potentially exceed 100 Gb/s. This enables us to meet the stringent requirements for next generation processing and communication platforms for higher communication and processing speed and denser on-chip integration. Therefore, the availability of such a material and device technology will have a major impact on next generation computing and communication systems.

Recently, graphene has been integrated on Si waveguide-based structures, and optical modulation has been demonstrated through electro-absorption effect [99-102]. Since these structures are waveguide-based, the footprint of the final modulator is large. There has also been reports of graphene integrated onto photonic crystal cavities, which are electrochemically tuned through ion gels [103, 104]. However, due to the low-speed nature of ion gels, they have not been able to demonstrate high speed modulation. Basically, smaller footprint photonic devices such as microring resonators with fast electrostatic gating scheme could result in higher speeds and denser integration.

The proposed graphene-SiN modulator in this work is electronically a simple graphene-based parallel-plate capacitor placed on top of SiN optical devices; therefore, under ideal circumstances, no current flows in DC, and the devices are ultra-low power. The phase shift and absorption change in graphene layers are induced through the change in the real and imaginary parts of the conductivity of graphene by applying voltage between the two graphene layers. Light-matter interaction takes place between carriers on the graphene sheet and the optical field inside the SiN devices. The required voltage/power

consumption of the modulator is determined by the strength of the electro-optic effect that is used for modulation. Recently a similar modulator based on hybrid graphene-SiN has been published [105]. Here, I use a much simpler fabrication process, and also use novel devices to show modulation on the hybrid graphene-SiN platform.

CHAPTER 2. DOUBLE-LAYER CRYSTALLINE SILICON ON INSULATOR MATERIAL PLATFORM

Here, I demonstrate a high-quality wafer-bonding technique to transfer a crystalline Si layer on top of an SOI substrate (with a thin SiO_2 interface in between) to form a high-quality material platform for integrated nanophotonics. The proposed process is based on oxide-oxide covalent bonding of two high-quality SOI wafer pieces at low temperatures. Using this process, I have shown that the optical loss of the resulting double-layer SOI (DLSOI) material can be reduced by one order of magnitude compared to existing results [27]. The quality of the developed DLSOI material is assessed by the fabrication of microring resonators and evaluating their Q's. I demonstrate Q's as high as 350k for microrings with 20 μm outer radius under TE polarization (i.e., electric field in the plane of the microring), which is the preferred polarization for applications such as modulation, switching, and reconfiguration of photonic devices. The evaluated intrinsic quality factor corresponds to the propagation loss of around 1.5 dB/cm. To the best of my knowledge, the Q's reported in this paper are the highest values for microrings fabricated on any DLSOI platform. The demonstrated material platform with high performance photonic resonators enables new optoelectronic and opto-mechanical device architectures for a wide range of applications such as optical modulation, interconnection, switching, light-matter interaction, and sensing.

2.1 Material Platform

The schematic of the DLSOI structure is shown in Figure 1(a), where a dielectric material (e.g., SiO_2) is sandwiched between two layers of Si. Figure 1(a) and Figure 1(b) show the field profiles of the fundamental modes of a single-mode waveguide in the DLSOI structure with TE (i.e., electric field parallel to the substrate) and TM (i.e., electric field normal to the substrate) polarizations, respectively (simulated using finite element method in COMSOL). As expected, the electromagnetic energy of the quasi-TE mode is primarily confined in the Si layers; therefore, the quasi-TE mode in this structure is useful for applications such as modulation and tunable devices where controlled charge accumulation in the two Si layers through the capacitive structure can be used to realize optoelectronic devices [106]. On the other hand, the electromagnetic energy of the quasi-TM mode of this structure is mainly confined in the interface layer, leading to a high field enhancement in the gap region. This makes the quasi-TM mode in this structure suitable for applications requiring light to interact with the material in the gap region for sensing [107] and nonlinear photonic applications [108]. Unless otherwise stated, throughout this dissertation, whenever I use the terms, TE and TM modes I mean quasi-TE and quasi-TE modes, respectively. Here, I primarily focus on TE polarization, which is the best choice for applications like modulation and switching based on charge accumulation in the $Si/SiO_2/Si$ capacitive structures (TM polarization usually becomes of interest when the SiO_2 layer is replaced by an active material, e.g., a nonlinear polymer).

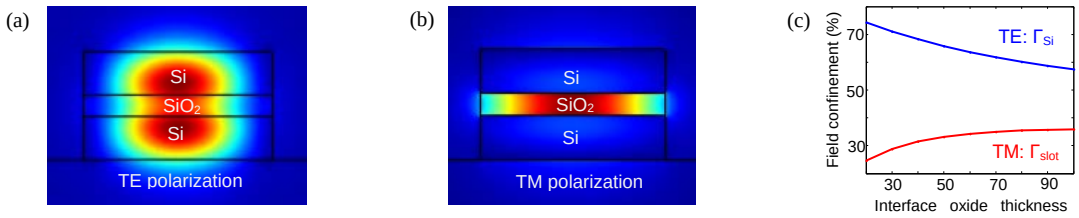

Figure 1 - (a) and (b) show the profile of the Poynting vector in the direction of propagation in a single-mode waveguide (waveguide width = 500 nm, Si layer thickness = 110 nm, interface oxide thickness = 60 nm) in the double-layer Si platform for the TE and TM polarizations, respectively. (c) Field confinement in the active region for TE and TM polarizations (defined as the ratio of the electric field energy in the active region to the total electric field energy.) Blue and red curves show the confinement in the Si and interface oxide layers for the TE and TM polarizations, respectively.

2.2 Fabrication

The DLSOI structure in this work is developed by bonding two single-crystalline SOI wafer pieces with a thin oxide interface in between. The oxide thickness for the devices presented in this paper is 60 nm, unless otherwise stated. To develop the DLSOI substrate ($Si/SiO_2/Si$ stack with thicknesses of 110nm/60nm/110nm), two SOI chips are oxidized with appropriate layer thicknesses (i.e., 30nm SiO_2 and 110nm Si) to be bonded together (Figure 2(a)). This is achieved through two steps; 1) thinning down the Si device layer of a commercial 6 inch SOI wafer (250 nm Si device and 3 µm buried-oxide (BOX) layers from Soitec, Inc.) by dry oxidation and oxide wet etching in buffered-oxide-etchant (BOE), and 2) using high-quality interface oxide growth (30 nm).

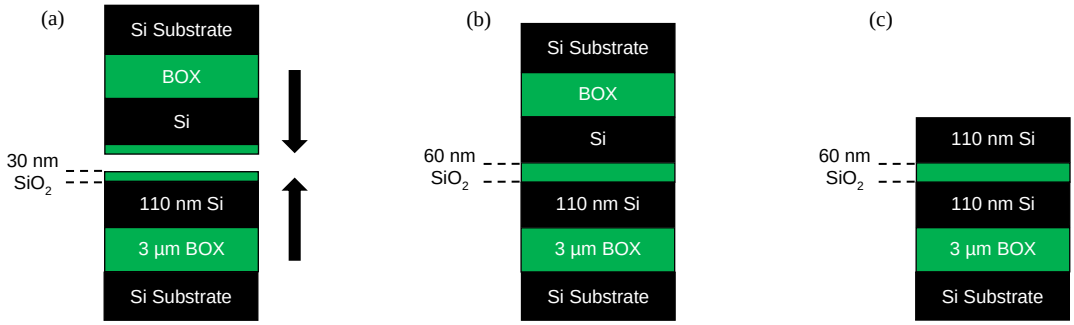

Figure 2 - Schematic of the bonding process steps: (a) two similar SOI chips with a thin oxide film are brought in contact after rigorous cleaning before bonding; (b) schematic of the bonded pair; (c) schematic of the bonded pair after removing the bulk Si and the BOX layers from the top SOI chip.

Making sure that the surface of the two chips that are to be bonded together stay clean and free of any particles during the whole process up to the point that they are brought in contact is very important. There are several steps that might introduce particles to the surface of the chips. For instance, during the cleaving step, if the top surface is not covered with a protective layer, cleaving dust and debris will attach to the surface. Figure 3 shows the top surface of a cleaved chip under dark field microscope which had not been covered during the cleaving process. As we can see, a lot of particles are introduced on the surface which make it unacceptable if it is to be used for high quality bonding.

Figure 3 - Surface of a Si chip after being cleaved without a protective layer on top of the chip.

In the thin-down step, after oxidation, the wafer is covered with Red First Contact-™ polymer (Photonic Cleaning Technologies) and cleaved into 1 by 2 inch chips. The polymer is used to protect the top surface from cleaving debris and is easily peeled off without leaving any residues after cleaving. After these steps the SOI chips are ready for the bonding process. Figure 4(a) shows an image of the protective polymer. Figure 4(b) shows a cleaved SOI wafer that is covered with the protective polymer before being cleaved into appropriate sizes.

(a)

(b)

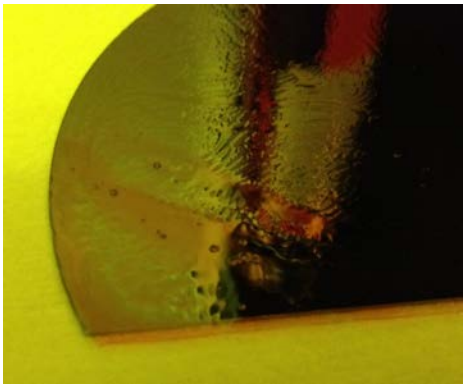

Figure 4 - (a) Red First Contact, the protective polymer; (b) surface of a wafer covered with First Contact.

To assure high-quality bonding, the prepared chips are rigorously cleaned followed by appropriate activation steps. The cleaning step starts with 30 min sonication in Acetone, Methanol and Isopropyl alcohol (AMI) (each twice) followed by a modified RCA process [109] in which, the chips are first immersed in SC-1 solution (H_2O:NH_4OH:H_2O_2 5:1:1) at 75º C for 20 minutes, rinsed with DI water, then immersed in SC-2 solution (H_2O:HCl:H_2O_2 6:1:1) at 75º C for 20 minutes, rinsed with DI water, and finally blow-dried with N_2. The AMI cleaning is very effective in removing most of the particles that might have ended up on the samples. Figure 5 shows the efficacy of the AMI clean on a cleaved piece of Si wafer. Figure 5(a) is the dark field micrograph of the piece before going through the AMI cleaning step, and Figure 5(b) is the dark field micrograph of the piece after being cleaned using AMI. As Figure 5(b) shows the Si chip is almost spotless after the AMI cleaning step.

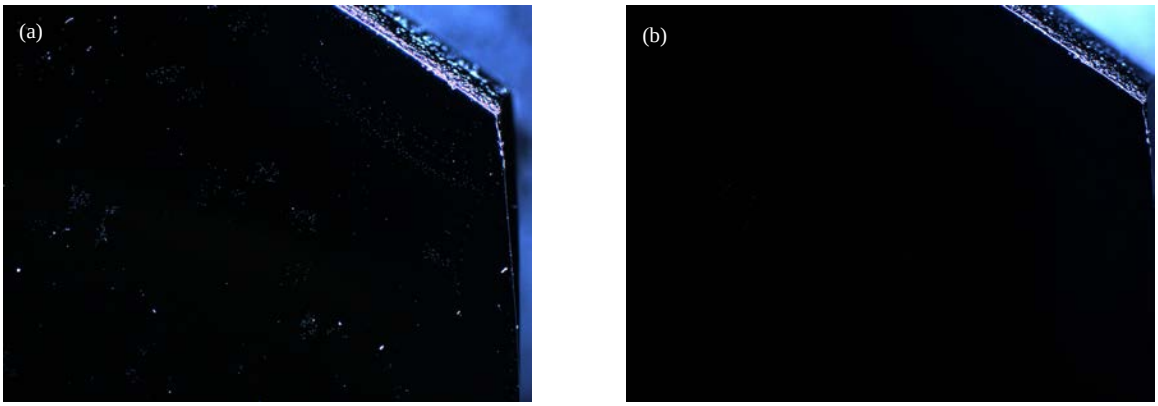

Figure 5 - A cleaved piece of Si wafer (a) before and (b) after going through the rigorous AMI cleaning.

High-quality quartz beakers are used during SC-1 and SC-2 to reduce contamination from alkali metals from ordinary glassware [109]. Figure 6 shows an image

of the Teflon carrier with two pieces that are to be bonded inside a quartz beaker. Teflon will not react with any of the acids or bases that are used during the bonding process.

Figure 6 - Teflon wafer carrier used to hold the pieces during the cleaning steps.

The activation steps are imperative to enable low-temperature wafer bonding, and are performed by first 30 seconds exposure to O_2 plasma in a reactive ion etching (RIE) tool [110] (Plasma-Therm RIE system, O_2 flow rate = 100 sccm, chamber pressure = 100 mTorr, and RF power = 200 W), followed by immediately dipping the chips in NH_4OH to render the surfaces more hydrophilic [111]. Then, the chips are blow-dried with N_2 and placed in contact with each other, and bonded (Figure 2(b)) in a Karl Suss SB6 bonder. Figure 7 shows an image of the Karl Suss SB6 wafer bonder used in this work. The bonding process is carefully optimized to achieve the highest bonding strength. The razor-blade test [112] is used to qualitatively measure the bonding strength. After placing the bonding pair inside the bonder chamber, the bonder chamber is evacuated down to 5×10-5 mbar, followed by slowly ramping up the bonding pressure to 4 bars at room temperature. After 30 minutes, the bonder temperature is also ramped up to 450º C and the bonding pair is

held under these conditions (pressure = 4 bars and temperature = 450º C) for 6 hours to increase the bonding strength. During all of the previous steps, from sample preparation to bonding, the SOI chips are only handled from the back side using a vacuum tweezer without touching their top surfaces to prevent contamination. Figure 8 shows an image of the vacuum tweezer (Waferpik from TDI) used in this work.

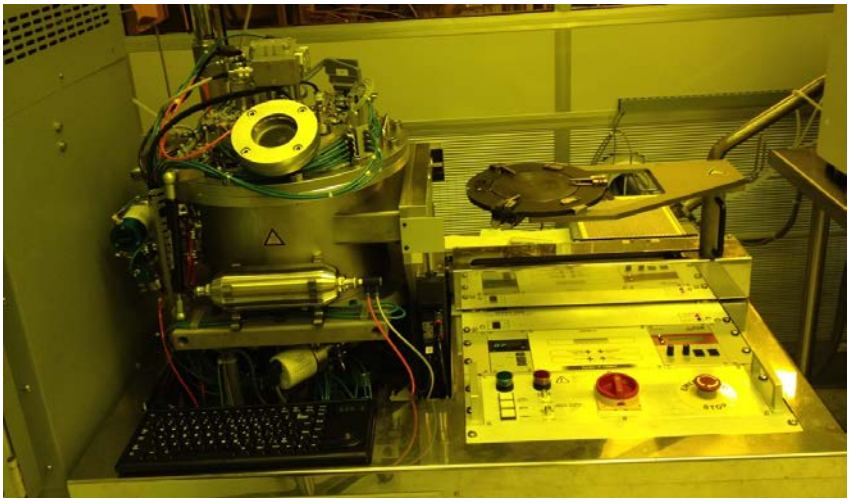

Figure 7 - An image if the Karl Suss SB6 wafer bonder.

(a)

(b)

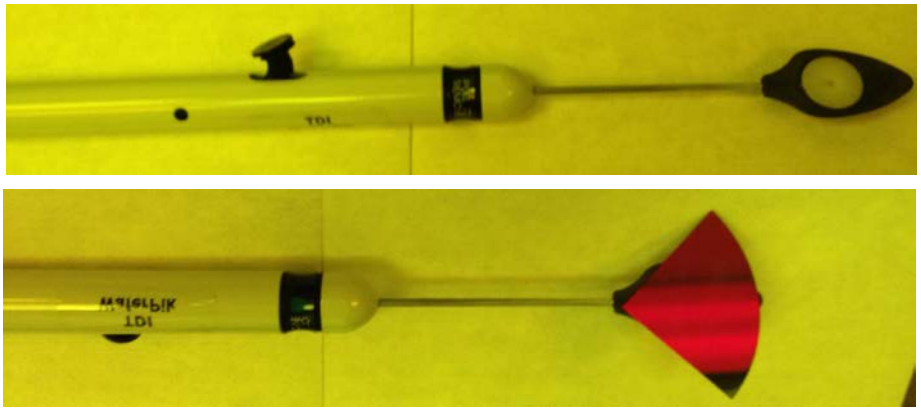

Figure 8 – The vacuum tweezer used for handling the pieces.

After successful bonding, the bulk Si and the BOX layers of the top SOI chip are removed using the Bosch process and BOE wet etching, respectively (Figure 2(c)). After

preparing the DLSOI platform, the optical devices are patterned using electron-beam resist hydrogen silsesquioxane (HSQ). The top and bottom Si layers of the devices are etched using Cl_2 gas in an STS inductively coupled plasma (ICP) system, and the 60 nm dry oxide interface is etched using CHF_3/Ar gas combination in an Oxford RIE system. Afterwards, the devices are coated with flowable oxide (FOx®-16 from Dow Corning) as the top cladding material.

Figure 9(a) shows a scanning-electron-microscope (SEM) image of the cross-section of a cleaved waveguide in the developed DLSOI platform. The thickness of the top and bottom Si layers is 110 nm, and the thickness of the interface SiO_2 is 60 nm. Figure 9(b) shows the top-view SEM image of a 2 μm radius microring, which is critically coupled to a bus waveguide.

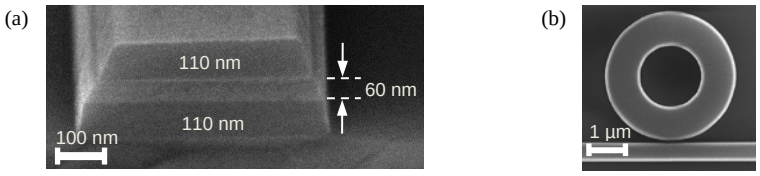

Figure 9 - (a) SEM image of the cleaved facet of a waveguide on the DLSOI at a 60 degrees tilt angle. The thickness of the two Si layers is 110 nm each, and that of the interface oxide layer is 60 nm; (b) top view SEM image of a 2 μm radius microring fabricated on the DLSOI platform.

2.3 Experimental Results and Discussion

To assess the optical quality of the DLSOI platform and hence the quality of the bonding process, I fabricated different resonators and measured their Q's. Microrings with a wide range of radii from 2 μm to 20 μm coupled to bus waveguides are fabricated on the DLSOI platform. The fabricated resonators are then characterized by measuring the

transmission spectra of the waveguides. Most of the resonance-based structures studied in this paper are based on the straight waveguide-resonator coupling scheme (as the one in Figure 9(b) and Figure 10(b)). In contrast, the waveguide-resonator coupling for the structure corresponding to Figure 11(d) is based on pulley coupling architecture, which is designed to selectively excite the fundamental radial TM mode of the resonator [71]. The width of waveguides in all cases is either 500 nm or 550 nm, and the gap between the waveguides and the resonators is adjusted between 100 nm to 550 nm to achieve critical coupling. Characterization of the fabricated devices is done using a swept-wavelength transmission characterization setup near 1550 nm wavelength. A fiber polarization controller is used to adjust the input polarization for the characterization. Tapered fibers are used to couple light into and out of the cleaved facets of the bus waveguides. The output light is detected using a variable gain photo-receiver and sent to a computer through a data acquisition card.

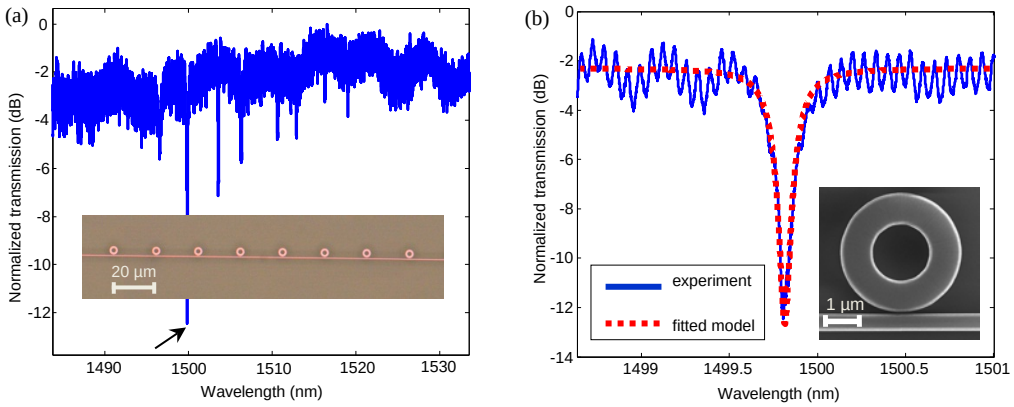

Figure 10 - (a) Transmission spectrum for an array of eight 2 μm radius microrings with different waveguide-resonator gaps for the TE polarization. The inset shows the optical image of the characterized resonator array. The waveguide width is 500 nm, and the waveguide-cavity gap starts from 125 nm for the leftmost resonator and increases in 25 nm increments, so that the rightmost resonator has a 300 nm gap. (b) The transmission spectrum for the resonance marked in (a) with a Q of 25k. Dashed

curve shows a Lorentzian resonance fitted to the experimental data. The inset shows the SEM image from one of the 2 μm radius microrings in the array.

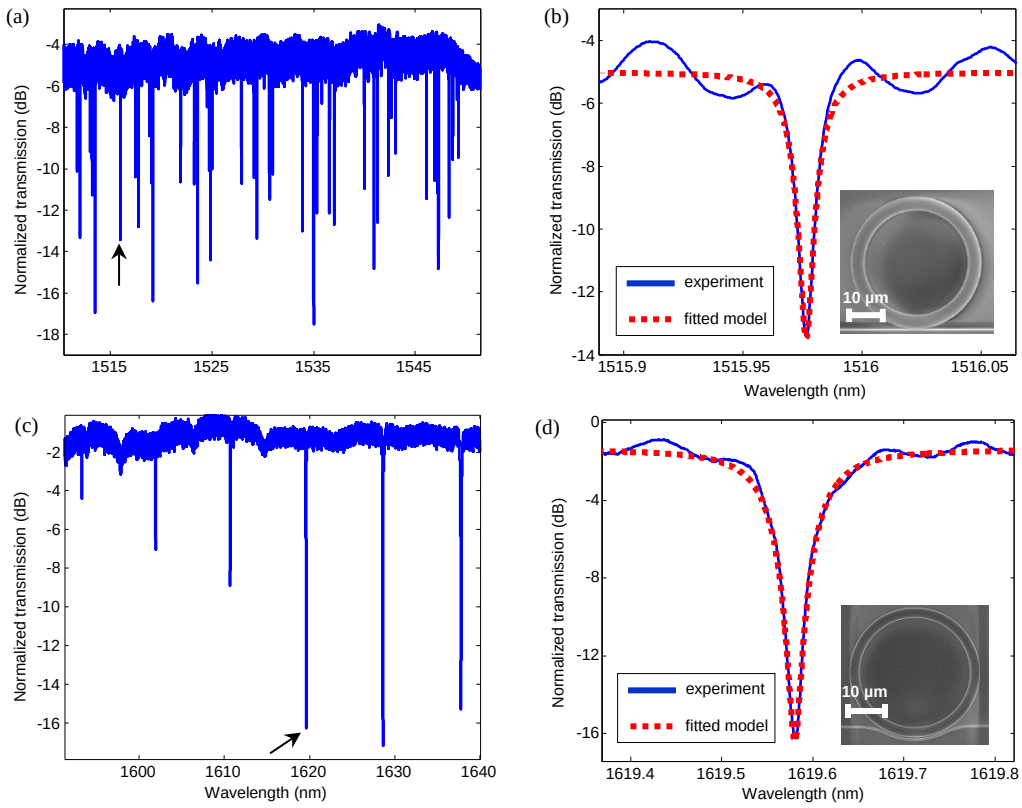

Figure 11 - (a) Transmission spectrum for a 20 μm radius multimode microring (ring width = 4 μm) for the TE polarization. The waveguide width is 550 nm, and the waveguide-cavity gap is 100 nm. (b) The transmission spectrum for the resonance marked in (a) with a Q of 350k. Dashed curve shows a Lorentzian resonance fitted to the experimental data. The inset shows the SEM image of one of the 20 μm radius multimode microring. (c) Transmission spectrum for a pulley coupled 20 μm radius multimode microring (ring width = 3 μm) for the for the TM polarization. The waveguide width, the pulley length, and the waveguide-cavity gap are 550 nm, 18.33 μm, and 535 nm, respectively. (d) The transmission spectrum for the resonance marked in (c) with a Q of 40k. The inset shows the SEM image of one of the pulley coupled 20 μm radius multimode microring. Dashed curve shows a Lorentzian resonance fitted to the experimental data.

Figure 10(a) shows the TE transmission spectrum (i.e., transmitted power through the bus waveguide divided by the incident power at different wavelengths) for an array of eight 2 μm radius microrings with different waveguide-resonator gaps from 125 nm to 300

nm (increments of 25 nm) to study different coupling regimes (i.e., over-, under-, and critical- coupling). The radius of each resonator is increased by 5 nm compared to the one to its left to avoid the overlap of resonance features. The width of the bus waveguide is 500 nm. Figure 10(b) shows the magnified plot of the transmission for one of the resonators that is close to critical coupling with an intrinsic Q of 25k. Dashed curve shows a Lorentzian resonance fitted to the experimental data. This is the first demonstration of a high-Q ultra-compact 2 μm radius microring on any double-layer Si platform. On the other extreme where size can be sacrificed for higher Q, I investigated the performance of 20 μm radius multimode microrings (ring width = 4 μm, waveguide width = 550 nm, and the waveguide-cavity gap = 100 nm). Figure 11(a) shows the TE transmission spectrum for this resonator with different radial order modes. Figure 11(b) shows the magnified plot for one of the high-Q modes with intrinsic Q of 350k. This is one order of magnitude higher than the previous reported result [27] and is the highest reported Q on any DLSOI platform to-date.

Figure 11(c) shows the TM transmission spectrum for a 20 μm radius multimode microring in which the resonator is pulley coupled to excite only its fundamental TM mode. Figure 11(d) shows the transmission spectrum for one of the high-Q TM modes with a Q of 40k. The considerable difference between the intrinsic Q's of the TE and TM modes (e.g., highest Q of 350k, and 40k, respectively for a 20 μm radius microring) can be attributed to different phenomena. First, the lower effective index of the TM mode results in higher radiation loss, specifically for higher order modes and the smaller resonators. At the same time, the by-product of hydrophilic bonding process is water molecules at the interface which will cause voids during annealing [113]. As seen in Figure 1(b), the

electromagnetic field is very strong at the interface for the TM mode, and its interaction with these interfacial voids would also contribute to the overall loss in the TM mode. Nevertheless, these voids can be removed using high temperature annealing [113], adding outgassing channels [113], or removing the interface oxide after bonding and refilling it with high quality (void-less) oxides using atomic layer deposition [114] to effectively increase the intrinsic Q of the TM modes.

Figure 12 shows the variations in the intrinsic Q of the TE modes of different microrings as a function of their outer radii. The width of the microrings with 2-3 µm, 5 µm, 10 µm, and 20 µm radii are 1 µm, 1.25 µm, 3 µm, and 4 µm, respectively. As it is clear from Figure 12, the resonator Q increases by increasing the resonator size.

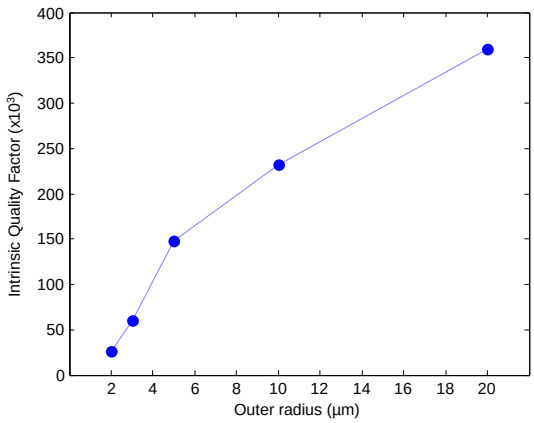

Figure 12 - The highest measured Q for TE polarization vs. the outer radius of the microrings fabricated in the DLSOI platform. The width of each microring is large enough to make sure that the intensity of fundamental TE-mode at the inner side-wall is negligible (i.e., the mode acts similar to a microdisk mode).

The Q's of the TE mode reported here for the DLSOI microrings are similar to those we achieve in single-layer Si structures (i.e., conventional SOI) using the same fabrication processes. This clearly shows that the proposed bonding process does not

increase the material loss (e.g., due to scattering). Furthermore, it enables 3-D integration to achieve sophisticated functionalities that are very hard to achieve in single-layer Si. For instance, microdisk electro-optical modulators can be fabricated in this platform, in which the top and bottom Si layers serve as the capacitor plates (where charge is accumulated), and the resonance wavelength of the device is modulated by carrier dispersion. Alternatively, electro-mechanically tunable photonic microdisk resonators can be realized by partially removing the interface oxide to allow mechanical displacement by applying voltage which leads to a large resonance wavelength shift. The operating voltage and the power dissipation of these devices will scale with dielectric thickness, which can be pushed to the lowest records using this bonding technique. Therefore, the modulation can be driven at low voltages, and switching will be rather low power and fast with no static power consumption, which can surpass the performance of state-of-the-art modulators based on reverse-biased PN-junction [115]. The polarization of interest in all these cases is TE, for which high-Q resonators were demonstrated here.

CHAPTER 3. POLARIZATION CROSS-COUPLING IN DOUBLE-LAYER SOI

In this chapter polarization cross-coupling between modes of microring resonators and waveguides due to structural asymmetries is investigated. I experimentally demonstrate the coupling between a double-layer SOI waveguide fundamental TM mode and microring higher-order radial TE modes.

3.1 Device Simulation

To understand the interaction between quasi-orthogonal modes, I place two double-layer SOI waveguides in close proximity and study the coupling between their quasi-orthogonal modes using the finite-element method (FEM) in COMSOL. The aim here is to see what the required conditions are to have efficient coupling between TE_0 of one waveguide and TM_0 (two quasi-orthogonal modes) of the other one. The double-layer SOI material platform used in this work is formed by bonding two SOI substrates with top and bottom Si thickness being 110 nm with 60 nm interface oxide in between [55].

The first requirement to have efficient cross-polarization coupling is for the two waveguides to be placed close enough for their quasi-orthogonal modes to have significant overlap; hence, the gap between the two waveguides is chosen to be 300 nm. The second major requirement is to make sure the two modes satisfy the phase matching condition, i.e., the effective refractive index of TE_0 of one, matches the effective refractive index of TM_0 of the other one. The widths of the waveguides are chosen accordingly (251.5 nm and 550 nm) to satisfy the phase matching condition at 1550 nm. In this case, since there is no

asymmetry in the structure, the non-dominant field components of each quasi-orthogonal mode are not strong enough to have significant coupling with the dominant field component of the mode, hence, there is no cross-polarization coupling. Figure 13(a) and Figure 13(b) show the mode profile of the resulting supermodes, in which no signs of TM_0 to TE_0 coupling is observed. This is better illustrated in Figure 13(c), i.e., the dispersion curve of TE_0 and TM_0 of each waveguide. As we can see, there is a crossing point between the dispersion curves of the two modes at 1550 nm which proves the lack of coupling between these two quasi-orthogonal modes.

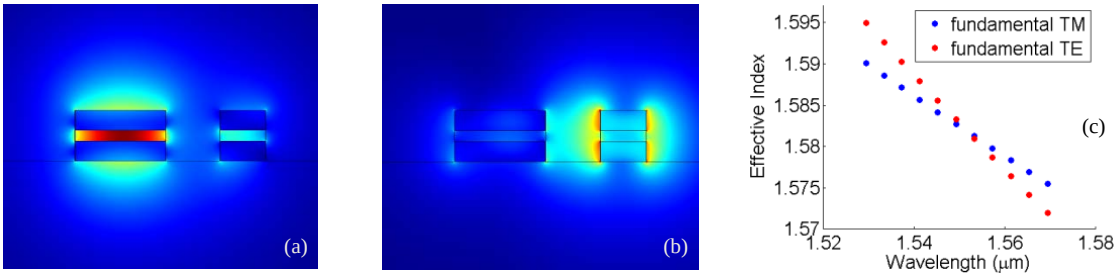

Figure 13 - Mode profile of the coupled coupled-waveguide structure (a) TM polarization and (b) TE polarization. (c) Dispersion of the coupled-waveguide structure with full symmetry. In (a)-(c) the thickness of top and bottom Si layers are 110 nm; the thickness of the interface oxide is 60 nm; the width of the left and the right waveguides and the gap between the waveguides are 550 nm, 251.5 nm, and 300 nm, respectively.

Next, I consider the case in which only the vertical symmetry is broken. The thickness of the top Si layer (90 nm) is thinner than that of the bottom Si layer (110 nm). The width of the interface oxide and the gap between waveguides are still 60 nm and 300 nm, respectively. To satisfy the phase matching condition under these new dimensions, the width of the waveguides are chosen 550 nm and 243.75 nm, respectively. As we can see in the mode profiles of the resulting structure in Figure 14(a) and Figure 14(b) and also from the crossing point in the dispersion curves in Figure 14(c), it is clear that breaking only the

vertical symmetry is not sufficient to get coupling between TM_0 and TE_0 of the two waveguides.

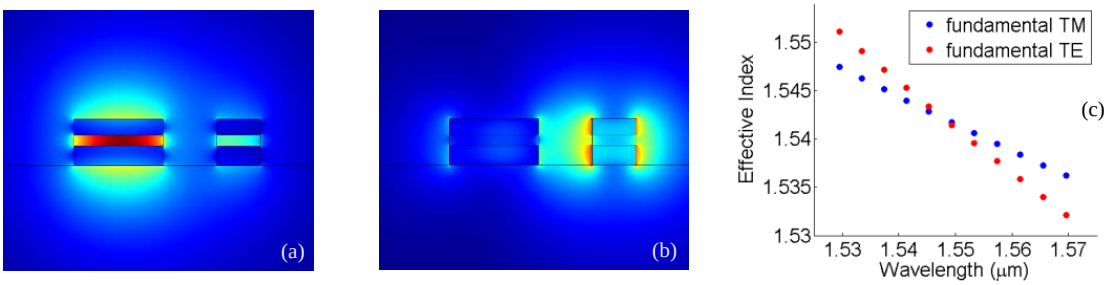

Figure 14 - Mode profile of the coupled coupled-waveguide structure (a) TM polarization and (b) TE polarization. (c) Dispersion of the coupled-waveguide structure with only vertical asymmetry. In (a)-(c) the thickness of top and bottom Si layers are 90 nm and 110 nm, respectively; the thickness of the interface oxide is 60 nm; the width of the left and the right waveguides and the gap between the waveguides are 550 nm, 243.75 nm, and 300 nm, respectively.

Next, I consider the case in which both vertical and horizontal symmetries in the waveguide structures are broken. This is achieved through removing small 25 nm by 110 nm rectangles from the two sides of the top Si layer of each waveguide (Figure 15(a) and Figure 15(b)). The width of the interface oxide and the gap between waveguides are still 60 nm and 300 nm, respectively. To satisfy the phase matching condition under these new dimensions, the width of the waveguides are chosen 550 nm and 273.8 nm, respectively. It is clear from the mode profiles of the structures (Figure 15(a) and Figure 15(b)) that hybrid super-modes exist and the fundamental TM mode of the left waveguide is coupled to the fundamental TE mode of the right waveguide. This is further evident from the anti-crossing between the dispersion curves of the TE_0 and TM_0 of the two waveguides (Figure 15(c)). Here, due to the induced vertical and horizontal asymmetries, the non-dominant components of the fields of each waveguide are strong enough to efficiently overlap with

the dominant components of the fields of the other waveguide to enable coupling between the two quasi-orthogonal modes (TM_0 and TE_0).

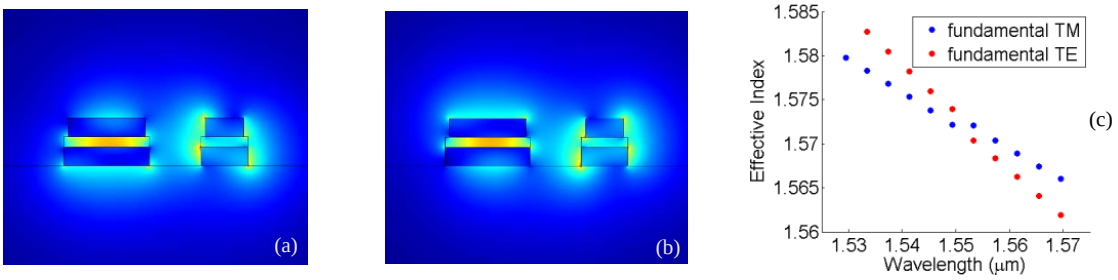

Figure 15 - (a)-(b) Mode profiles of the hybrid supermodes. The TM_0 of the left waveguide is coupled to the TE_0 of the right waveguide. (c) Dispersion of the coupled-waveguide structure with both vertical and horizontal asymmetries. In (a)-(c) the thickness of top and bottom Si layers are 110 nm while 25 nm by 110 nm rectangles are removed from the edges of top Si layer; the thickness of the interface oxide is 60 nm; the width of the left and the right waveguides and the gap between the waveguides are 550 nm, 273.8 nm, and 300 nm, respectively.

With asymmetries present in the double-layer SOI platform, one can also couple the fundamental modes to higher order modes. Here I study the case of coupling the fundamental TM mode of one waveguide to the tenth TE mode of the other one. As I showed for the case of coupling TE_0 and TM_0, by having perfect symmetry this cross-polarization would not be possible, so I will only consider two cases with structural asymmetries present.

First, I consider the case with only vertical asymmetry. The thickness of the top Si layer 20 nm thinner than the bottom Si layer (90 nm versus 110 nm). The width of the interface oxide and the gap between waveguides are still 60 nm and 300 nm, respectively. To satisfy the phase matching condition under these new dimensions, the width of the waveguides are chosen 3660.75 nm and 550 nm, respectively. As we can see in the mode profiles of the resulting structure in Figure 16(a) and Figure 16(b) and also from the anti-

crossing in the dispersion curves in Figure 16(c) the coupling of the TE_{10} mode and the TM_0 mode under vertical-only asymmetry is possible here (in contrast to TE_0/TM_0 coupling in Figure 13) since these modes have the same parity which result in nonzero overlap between them in the absence of horizontal asymmetry.

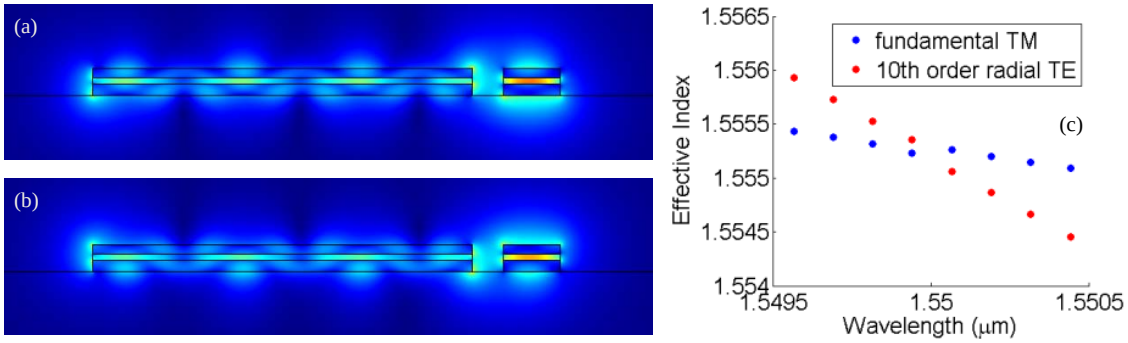

Figure 16 - (a)-(b) Mode profiles of the hybrid supermodes. The TM_0 of the right waveguide is coupled to the TE_{10} of the left waveguide. (c) Dispersion of the coupled-waveguide structure with only vertical asymmetry. In (a)-(c) the thickness of top and bottom Si layers are 90 nm and 110 nm, respectively; the thickness of the interface oxide is 60 nm; the width of the left and the right waveguides and the gap between the waveguides are 3660.75 nm, 550 nm, and 300 nm, respectively.

Figure 17 shows the case with both vertical and horizontal symmetries broken through removing small 25 nm by 110 nm rectangles from the two sides of the top Si layer of each waveguide (Figure 17(a) and Figure 17(b)). The width of the interface oxide and the gap between waveguides are still 60 nm and 300 nm, respectively. To satisfy the phase matching condition under these new dimensions, the width of the waveguides are chosen 3623.5 nm and 550 nm, respectively. It is clear from the hybrid supermodes in Figure 17(a) and Figure 17(b) and also from the anti-crossing in the dispersion curves in Figure 17(c) that the TE_{10} and the TM_0 are coupled here.

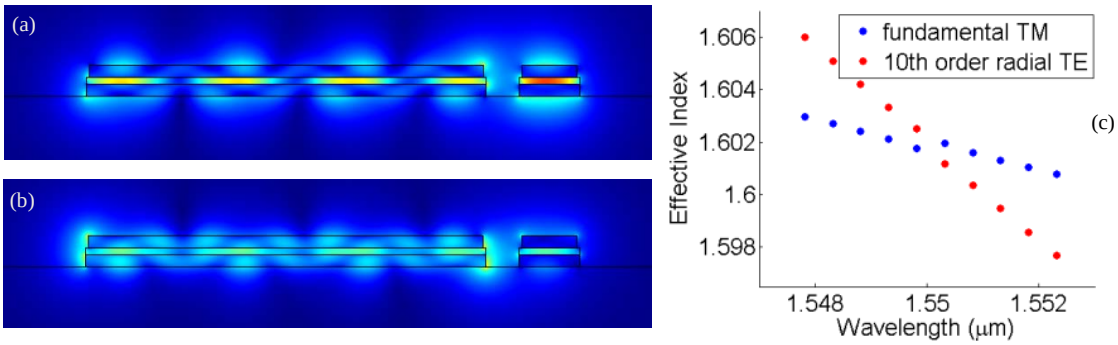

Figure 17 - (a)-(b) Mode profiles of the hybrid supermodes. The TM0 of the right waveguide is coupled to the TE10 of the left waveguide. (c) Dispersion of the coupled-waveguide structure with only vertical asymmetry. In (a)-(c) the thickness of top and bottom Si layers are 90 nm and 110 nm, respectively; the thickness of the interface oxide is 60 nm; the width of the left and the right waveguides and the gap between the waveguides are 3660.75 nm, 550 nm, and 300 nm, respectively.

3.2 Fabrication

To experimentally observe this phenomenon, I use a coupled waveguide-microring structure in double-layer SOI prepared using high-quality wafer bonding. Replacing one of the waveguides with a microring will enhance the polarization coupling efficiency and therefore, directional couplers with long tapers would no longer be necessary. The structures are patterned using electron-beam resist hydrogen silsesquioxane (HSQ). The devices are fully etched using Cl_2 gas in a Plasma-Therm inductively coupled plasma (ICP) system. Afterwards, the devices are coated with flowable oxide (FOx®-16 from Dow Corning) as the top cladding material. Figure 18(a) shows an SEM of the cross-section of a double-layer SOI waveguide. I fabricate 20 μm radius multimode microrings (4 μm width) coupled to 550 nm wide waveguides (100 nm coupling gap) in the double-layer SOI material platform to experimentally demonstrate polarization coupling between the TM_0 mode of the waveguide and the TE_{10} of the microring. An SEM image of a fabricated structure is shown in Figure 18(b). Asymmetries similar to those used for simulations

(Figure 17(a) and Figure 17(b)), which are essential for successful cross-polarization coupling, are induced during the fabrication process using just a single step etch. The edges of the top Si layer are etched more heavily than those of the bottom Si due to the consumption of the oxide based e-beam resist (HSQ) during the etch process.

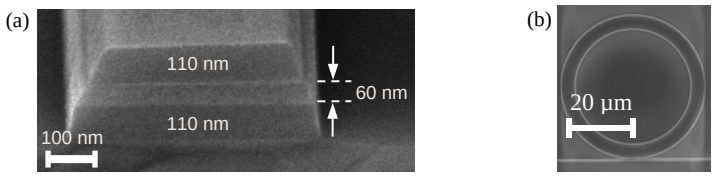

Figure 18 - (a) SEM image of the cleaved facet of the asymmetric waveguide on the double-layer SOI; (b) top view SEM image of a 20 µm radius microring (4 µm width) coupled to a 550 nm wide waveguide (waveguide-ring gap is 100 nm) fabricated on the double-layer SOI platform.

3.3 Experimental Results

Characterization of the fabricated devices is done using a swept-wavelength transmission characterization setup. A fiber polarization controller is used to adjust the input polarization for the characterization. Tapered fibers are used to couple light into and out of the cleaved facets of the bus waveguides. The output light is detected using a variable gain photo-detector and sent to a computer through a data acquisition card. Figure 19(a) shows the transmission spectrum of a 20 µm microring excited by coupling TM-polarized light into the waveguide using tapered fibers. As we can see in Figure 19(b) signatures of four different family of modes are present in the spectrum. By performing in-depth FEM simulations for different radial order modes of a 4 µm wide microring, the results of which are shown in Figure 19(c)-(f), the four different family of modes are identified as follows: the first order radial TM mode with free spectral range (FSR) of around 8.45 nm (red), the second order radial TM mode with FSR of around 8.6 nm (cyan), the ninth order radial TE

mode with FSR of around 5.1 nm (black), and the tenth order radial TE mode with FSR of around 4.8 nm (green).

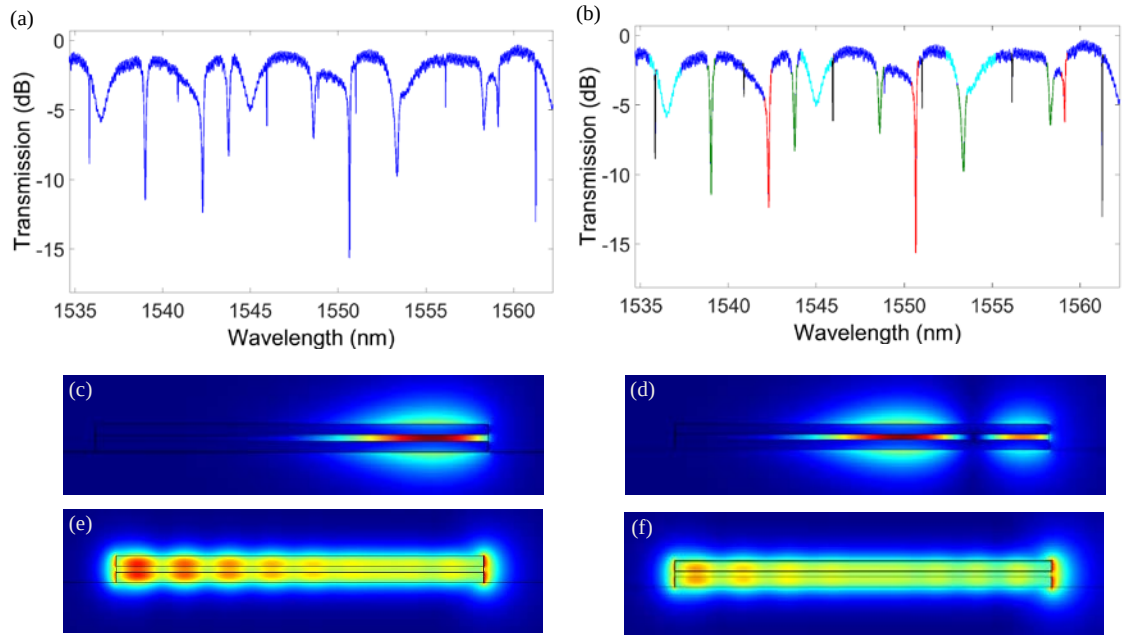

Figure 19 - Transmission spectrum of a 20 µm radius microring (4 µm width) coupled to a 550 nm wide waveguide (waveguide-ring gap is 100 nm) fabricated on the double-layer SOI platform excited by the fundamental TM mode of the waveguide. (b) The same as (a) with four different family of modes identified. Mode profile of the (c) first order radial TM mode FSR of around 8.45 nm; (d) second order radial TM mode with FSR of around 8.6 nm; (e) ninth order radial TE mode with FSR of around 5.1 nm; (f) tenth order radial TE mode with FSR of around 4.8 nm.

3.4 Discussion

Since the input waveguide is excited by the TM-polarized laser light, signatures of the first two radial order TM modes of the microring are to be expected in the transmission spectrum. However, the TE_9 and TE_{10} are only excited due to the induced asymmetries (through the etching process) in the structure. This is, to the best of my knowledge, the first

demonstration of the coupling of a waveguide mode to such high order resonator modes with quasi-orthogonal polarization.

If we want to have just the TE resonances of the microring while exciting it with the TM mode of the input waveguide, we can use an add/drop configuration as shown in Figure 20(a). The radius of the microring is 20 μm (4 μm width); the through port waveguide width and gap are 550 nm and 100 nm, respectively; and the drop port waveguide width and gap are 200 nm and 100 nm, respectively. The transmission spectrum of the drop port, while the through port is excited with TM polarized-light, is shown in Figure 20(b). Here, the signatures of only two family of modes (TE_9 with sharper resonances and TE_{10} with wider resonances) are present, and we no longer see any signatures corresponding to TM modes of the microring. This is achieved through having the width of the drop port narrow enough (200 nm) not to support any TM modes, whereby having only TE modes present at the drop port.

For applications in which we do not want to have any polarization cross-coupling, there are two options available. One is to etch the devices in a more anisotropic process to have less asymmetries in the final structures. Or to use pulley-coupled designs to selectively excite only the TM mode of the microring. Figure 20(c) shows the Optical micrograph of a pulley-coupled 20 μm radius multimode microring (ring width 3 μm). The bus waveguide width, the pulley length, and the waveguide-cavity gap are 550 nm, 18.33 μm, and 535 nm, respectively. In Figure 20(d) we see the transmission spectrum of the pulley-coupled microring with only TM_1 resonances of the microring excited by the fundamental TM mode of the input waveguide.

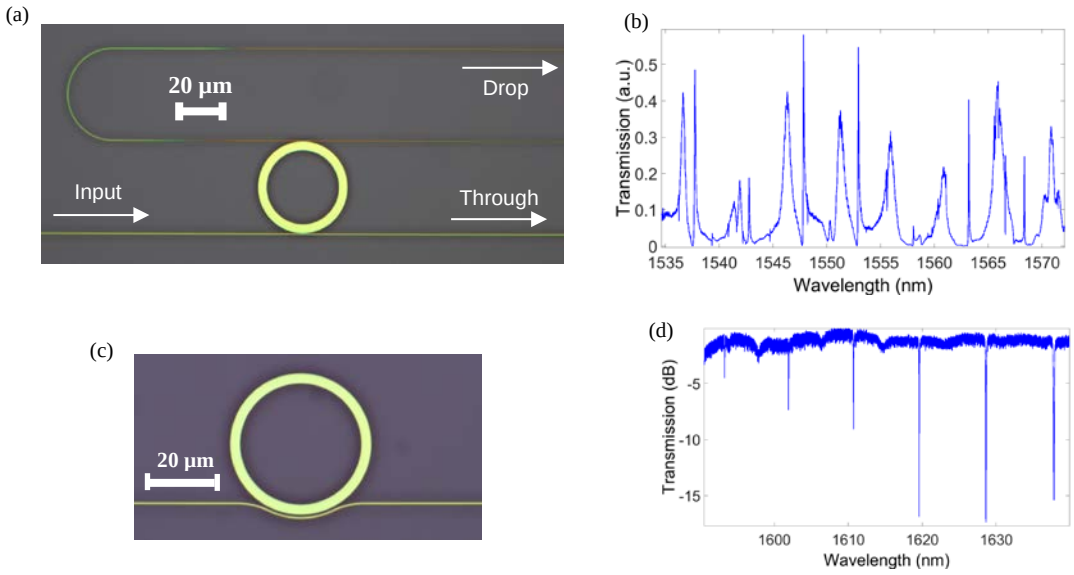

Figure 20 - (a) Optical micrograph of an add-drop filter. The microring radius is 20 µm (4 µm width). The through port waveguide width and gap are 550 nm and 100 nm, respectively. The drop port waveguide width and gap are 200 nm and 100 nm, respectively. (b) Transmission spectrum of the drop port of the add/drop filter with TE9 and TE10 resonances of the microring excited by the fundamental TM mode of the through port waveguide. (c) Optical micrograph of a pulley-coupled 20 µm radius multimode microring (ring width = 3 µm). The waveguide width, the pulley length, and the waveguide-cavity gap are 550 nm, 18.33 µm, and 535 nm, respectively. (d) Transmission spectrum of the pulley-coupled microring with only TM1 resonances of the microring excited by the fundamental TM mode of the input waveguide.

In summary, I studied cross-polarization in double-layer SOI platform. I showed that due to unique asymmetries present in this structure fundamental TE and TM modes can be coupled together with only a single step etch. I experimentally demonstrated coupling between the fundamental TM mode of the waveguide to the 9^{th} and 10^{th} TE radial order modes of a microring resonator. This is the first time such cross-polarization coupling to such high order modes are demonstrated. I used an add/drop filter to demonstrate polarization rotation from TM to higher radial order TE modes. Overall, the results suggest

that the double-layer SOI platform and the unique asymmetries associated with it could be a promising candidate to perform polarization manipulations and rotations.

CHAPTER 4. ULTRA-COMPACT HIGH-Q SIN RESONATORS

As discussed in section 1.2.1, in order to address issues with the SOI platform for integrated photonics applications (such as optical loss at visible wavelengths, high nonlinearity, and power handling), SiN has been suggested as a new versatile platform. However, SiN is not perfect itself. For example, due to the lower index contrast of SiN platform, high-Q ultra-small SiN-based microdisk resonators that are required for dense integration of optical systems have not been realized yet. In this chapter I will address this issue using a two prong approach. Through using a relatively thick SiN film and over-etching the bottom oxide substrate to reduce the radiation loss of the devices, I have enabled miniaturized high-Q microdisk resonators. In the rest of this chapter, I will first discuss my approach in detail followed by experimental results and final discussion.

4.1 Device Simulation

As mentioned earlier, in this work, a relatively thick LPCVD SiN film is used to fabricate the devices. The thicker the SiN film, the higher the effective index of the modes. Figure 21 shows the field profile for the fundamental TE-like modes of three waveguides (SiN on SiO_2) at 772 nm wavelength. All simulations in this chapter are performed using the finite-element method (FEM) in COMSOL at or near 772 nm wavelength. The width of all three waveguides is 600 nm. The SiN film thickness is 200 nm for Figure 21(a), 300 nm for Figure 21(b), and 400 nm for Figure 21(c), with effective refractive indices of 1.6143, 1.7219, and 1.7809, respectively. As expected the waveguide with the thickest film results in the highest index and provides the highest field confinement. One could argue that thinner films could potentially provide similarly high effective refractive indices if a

wider waveguides are chosen. However, this is at the expense of losing on density and device footprint.

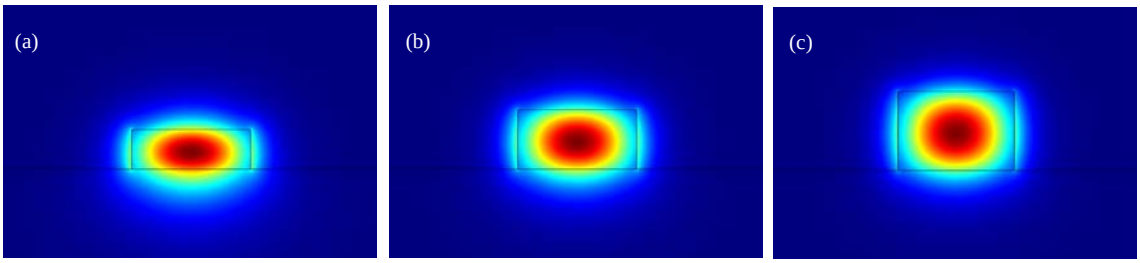

Figure 21 - Fundamental TE-like mode profile of a SiN on SiO2 waveguide. The SiN thickness is 200 nm in (a), 300 nm in (b), and 400 nm in (c). The waveguide width is 600 nm for all three waveguides and the top cladding is air.

The thickness of SiN film is chosen at 400 nm, as films thicker than this are prone to crack formation due to increasing tensile stress, which cause unacceptable high scattering loss, whereby limiting the Q [64, 116, 117]. There have been reports on methods for mitigating crack formation in thicker SiN films, including temperature cycling and annealing during growth, multistep growth with cooling cycles in between, and placing stress relief sites on the wafer before growth [64, 117, 118]. Although these methods can be applied to grow thicker SiN films, working with thicker films has another drawback which lead me to set 400 nm as the upper limit for the thickness of SiN films in this work. The issue is controlling the waveguide-resonator gap. Dry etching processes for photonic structures on SiN are usually developed to minimize the sidewall roughness and tend to have limited anisotropy. This results in etched waveguide-resonator gaps in SiN platform to end up considerably wider than the original layout. As I will discuss later, I etch an extra 200 nm of the bottom SiO_2 cladding (to increase the index contrast) which is etched together along with the SiN film. That is why, to end up with a range of acceptable gaps to

enable different coupling regimes, for this work, SiN films with up to 400 nm thickness are deposited.

The second approach that I take to enable high-Q ultra-compact structures, is to over-etch the bottom SiO_2 cladding to distance the resonator modes away from leaky substrate modes, whereby reducing the radiation loss of ultra-compact resonators. Figure 22 shows how over-etching the oxide cladding underneath the SiN film moves the microdisk mode away from substrate leaky modes. The SiN film thickness is 400 nm and the disk radius is 2.5 µm. In Figure 22(a) the etching is assumed to have stopped right at the SiN/SiO_2 interface. But, in Figure 22(b) the SiO_2 cladding is assumed to have been over-etched by 200 nm. As we can see, the mode of the microdisk has better confinement in Figure 22(b) and as I will discuss next has a higher radiation Q due to reduced bending loss.

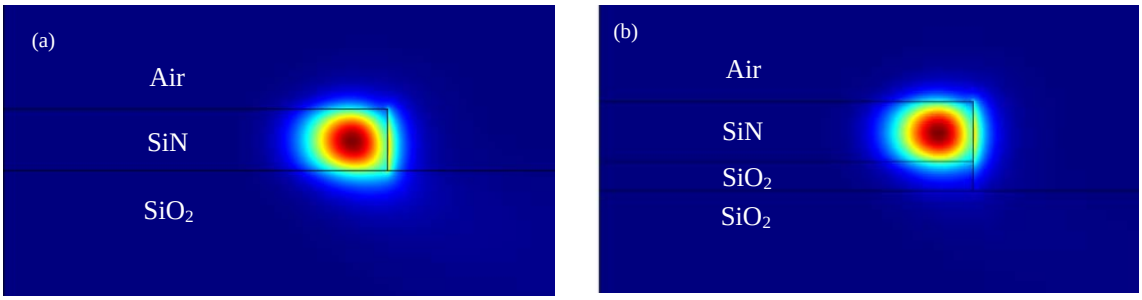

Figure 22 - First radial TE-like mode of a SiN on SiO_2 microdisk. The SiN thickness is 400 nm and the disk radius is 2.5 µm. The oxide bottom cladding is intact in (a) and over-etched by 200 nm in (b).

Figure 23, Figure 24, and Figure 25 show how the radiation Q of compact microdisk resonators change as a function of oxide cladding over-etch. For all three figures, the first radial TE-like mode of the microdisk is simulated near 772 nm. In Figure 23 the SiN film thickness and microdisk radius are 200 nm and 4.5 µm, respectively. In Figure 24 the SiN film thickness and microdisk radius are 300 nm and 3.5 µm, respectively. In Figure 25 the

SiN film thickness and microdisk radius are 400 nm and 2.5 µm, respectively. As seen in the figures, through over-etching the bottom oxide cladding the radiation Q is increased exponentially. For example, Figure 25 shows that over-etching the bottom cladding by 200 nm increases the radiation Q by more than an order of magnitude. In this case, the resonator Q will no longer be limited by radiation loss to the substrate (scattering loss will be the dominant loss).

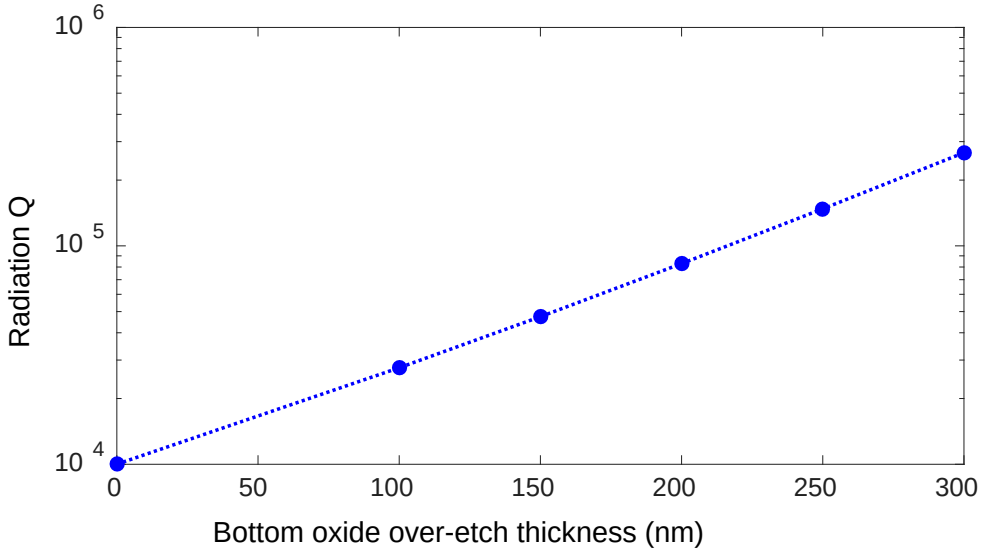

Figure 23 - Radiation Q simulation of the first radial TE-like mode of microdisk resonators as a function of bottom oxide cladding over-etch. The SiN thickness and microdisk radius are 200 nm and 4.5 µm. The top cladding is air.

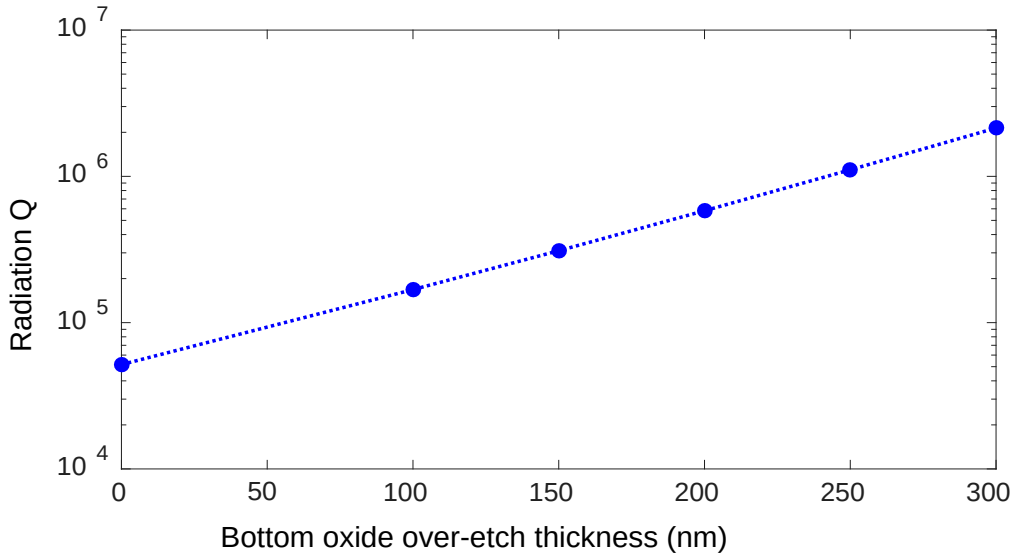

Figure 24 - Radiation Q simulation of the first radial TE-like mode of microdisk resonators as a function of bottom oxide cladding over-etch. The SiN thickness and microdisk radius are 300 nm and 3.5 µm. The top cladding is air.

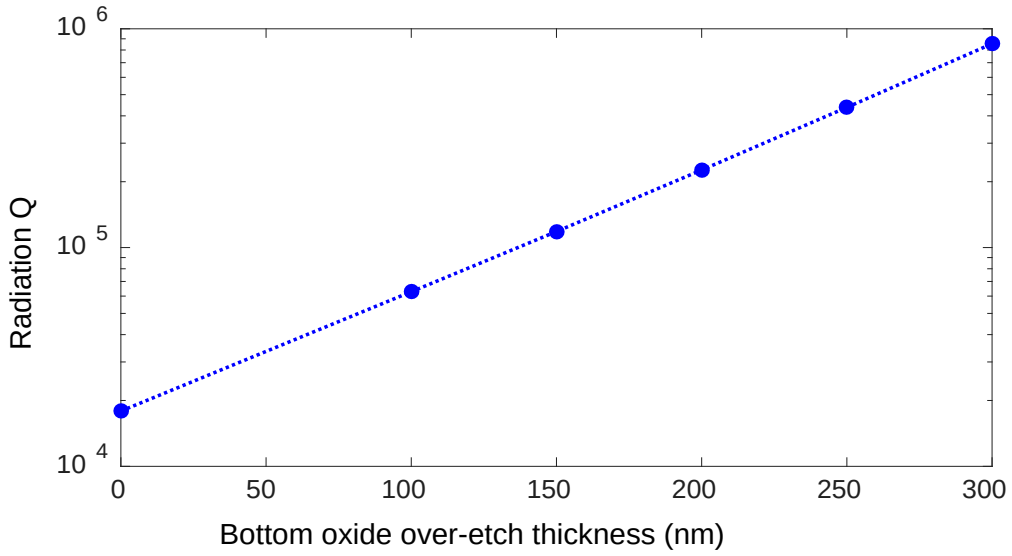

Figure 25 - Radiation Q simulation of the first radial TE-like mode of microdisk resonators as a function of bottom oxide cladding over-etch. The SiN thickness and microdisk radius are 400 nm and 2.5 µm. The top cladding is air.

We could also envision having some oxide just on top of the resonator. This extra oxide will make the resonator mode more symmetric and reduce the radiation loss through preventing the mode from leaking into the bottom oxide cladding. Figure 26 shows how the microdisk's TE-like mode becomes more symmetric though adding oxide to the top of the microdisk and having the oxide over-etched by some amount. In Figure 26(b), the bottom oxide cladding is over-etched by 100 nm, and 100 nm extra oxide is assumed to be on top of the microdisk, as compared to the case of no over-etching and no oxide on top of the resonator (Figure 26(a)). So, a combination of bottom cladding over-etching and having some amount of oxide on top of the microdisk could potentially result in ultra-compact resonators with higher radiation-limited Q's. I should note that the extra top oxide has to be only on top of the devices. Because, having any oxide on the sides will partially couple the mode to the bottom oxide cladding, whereby contributing to bending loss and defeating its purpose. Therefore, the top oxide has to be deposited on the SiN film before lithography, for example using methods like plasma-enhanced chemical vapor deposition (PECVD) or LPCVD.

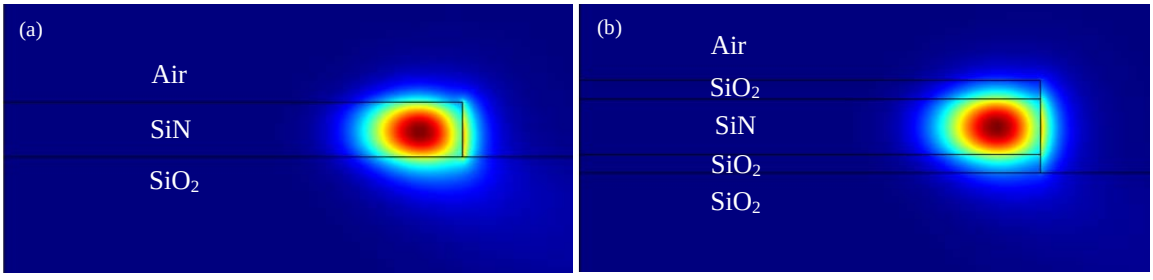

Figure 26 - First radial TE-like mode of a SiN on SiO_2 microdisk. The SiN thickness is 300 nm and the disk radius is 2.5 µm. No bottom oxide cladding over-etch and no extra oxide on top of the microdisk in (a) and 100 nm bottom oxide cladding over-etch and 100 nm extra oxide on top of the microdisk in (b).

Figure 27 shows how the radiation Q of compact microdisk resonators changes as a function of top oxide on the microdisk at three different oxide cladding over-etch depths. The first radial TE-like mode of the microdisk is simulated near 772 nm. The SiN film thickness and microdisk radius are 300 nm and 2.5 μm, respectively. Unlike for the case of oxide over-etch depth, which we saw to have an exponential effect on the radiation Q (Figure 25), the addition of the top oxide will only incrementally enhance the Q and even that enhancement saturates after a certain top oxide thickness. As an example from Figure 27, the radiation Q would be higher if 200 nm oxide bottom cladding is over-etched, versus etching only half (100 nm) and having another 100 nm oxide on top of the microdisk. Moreover, the quality of PECVD or LPCVD oxide films are inferior to the bottom oxide cladding (thermally grown). Having those kinds of oxide on top of the microdisk could potentially add to the overall optical loss through scattering. Therefore, in this work I only over-etch the oxide bottom cladding without adding any extra oxide on top of the microdisks.

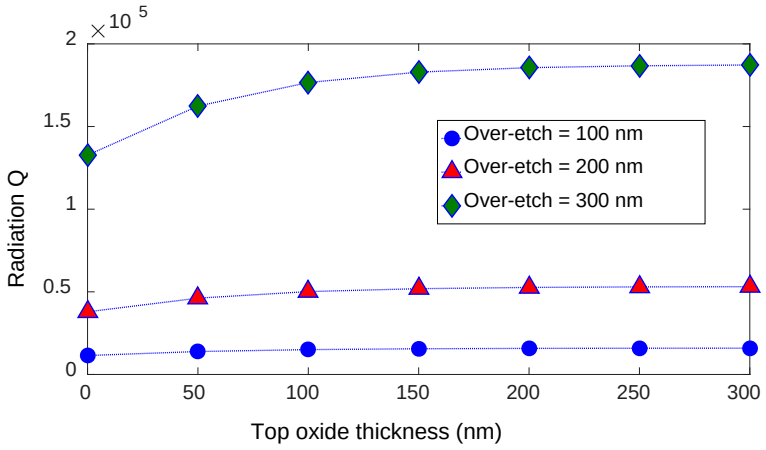

Figure 27 - Radiation Q simulation of the first radial TE-like mode of a microdisk resonator as a function of top oxide thickness for three different oxide over-etch depths. The SiN thickness and microdisk radius are 300 nm and 2.5 μm.

4.2 Fabrication

In this work, high quality stoichiometric LPCVD SiN is deposited on 4 μm thermally grown SiO_2 (as bottom cladding). Ultra-compact resonators with different radii are patterned the substrates; the SiN film is fully etched and, the bottom oxide cladding is etched at two different depths, 100 nm and 200 nm, to compare the intrinsic Q of the two cases. The oxide cladding over-etch depth is capped at 200 nm. Although Figure 23, Figure 24, and Figure 25 suggest that a deeper oxide over-etch would result in higher radiation Q's, the intrinsic Q of the resonators will be limited by scattering loss (e.g., from etched sidewalls) at such high radiation Q's. So, having a deeper oxide over-etch profile would not effectively increase the intrinsic Q of the microdisks, hence the over-etch depth is capped at 200 nm. Next I need to discuss the device etching process. So, as discussed, a process to enable etching a stack of 400 nm SiN and 100-200 nm SiO_2, with smooth sidewalls is required. Although there have been reports of etching thick SiN films (over 400 nm) using conventional electron-beam (e-beam) resists such as ma-N [64, 117-119] and thick HSQ (FOx-16) [120], due to the limited etch resistance of e-beam resists you cannot etch very deep profiles (over 1 μm) in SiN using them. I believe a hard mask could potentially allow much deeper etching profiles. On the other hand, while hard metal masks (e.g., Ni and Cr) could potentially be used to achieve the required etching selectivity, they limit the intrinsic Q of the resonators through scattering, due to the resulting rough sidewalls (caused by the large grain sizes of the evaporated metal). To resolve this issue, I have developed a two-step etching process based on using alumina (Al_2O_3) as hard mask to etch deep profiles onto SiN/SiO_2. First, alumina is patterned using a conventional e-beam resist then the patterned alumina will serve as hard mask to etch SiN/SiO_2.

The fact that SiN and SiO_2 are efficiently etched in fluorine-based plasma makes alumina an ideal mask for dry etching them. Because alumina provides excellent etch resistance in such plasma chemistries [121, 122]. The reason for that is that the resulting etch byproduct (AlF_3) is nonvolatile which inhibits effective dry etching of alumina in such plasma chemistries [122-125]. Moreover, to enable high-quality sidewalls (by avoiding large grain sizes), I use alumina deposited by atomic layer deposition (ALD), which provides a dense pinhole-free layer with ultra-fine grain sizes [126]. Unlike fluorine-based plasma, alumina is easily etched in chlorine-based plasma chemistries [127, 128]. So, after depositing alumina on the SiN wafers, it is first patterned in chlorine-based plasma then used as a hard mask to etch SiN and SiO_2 in fluorine-based plasma. Previously, the lift-off process has been used to pattern alumina as the hard mask [121]. However, the lift-off process is not reproducible, and might result in rough sidewalls.

As mentioned earlier, I believe dry etching alumina using chlorine-based plasma is the best approach to pattern it. Through careful optimization I have been able to develop a dry-etching process for alumina with minimal sidewall roughness which is necessary to enable high-Q resonators. Pure Cl_2 is not an effective gas to dry etch alumina due to the inability of Cl_2 to extract Oxygen. That is why I added BCl_3 to the gas mixture to help remove Oxygen in the form of BCl_xO_y byproducts [128] to increase the etch rate. In this work, alumina thin films are etched using BCl_3/Cl_2 gas mixture in an inductively coupled plasma (ICP). The etch rate and selectivity of alumina with respect e-beams are investigated as functions of the gas ratio and plasma RF powers (coil and platen). Finally, I used X-ray photoelectron spectroscopy (XPS) to make sure alumina films after being

exposed to the etching plasma maintain the Oxygen to Al ratio they had before etching. In the next section I will go over the details of the alumina etching process.

4.2.1 Developing Alumina as Etching Process

As discussed earlier, I started with a Chlorine-based plasma, namely BCl_3/Cl_2, to develop an alumina etching recipe. As a starting point I set chamber pressure to 5 mTorr, the coil power to 300 W, and gas flow rates at BCl_3/Cl_2 25/25 sccm. I then swept the platen power and measured the etch rate and selectivity with respect to NEB (Figure 28). The etch rate turned out to be around 35 nm/min which is a bit low. In the next step, I increased the coil power to get higher alumina etch rate and selectivity.

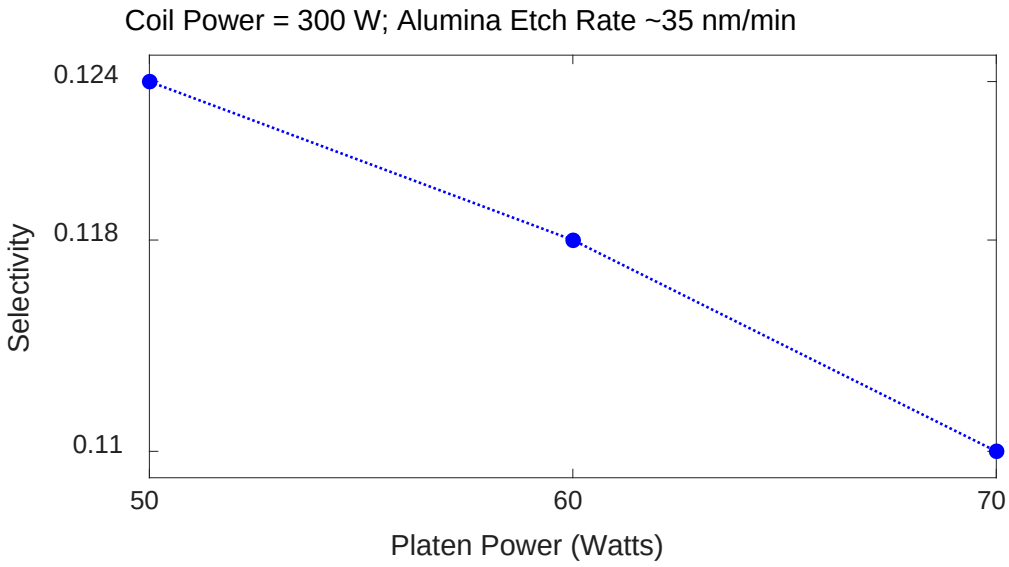

Figure 28 - Selectivity measurement with coil power set to 300 W. Platen power is swept.

The coil power was increased to 700 W. Once again, I swept the platen power. So, the chamber pressure was set to 5 mTorr, the coil power to 700 W, and gas flow rates at BCl_3/Cl_2 25/25 sccm. Once again, I measured the etch rate and selectivity with respect to

NEB (Figure 29). The etch rate turned out to be around 120 nm/min which is acceptable for my application. However, the selectivity is still a bit low. In the next step, I increased the coil power to 800 W to get higher selectivity.

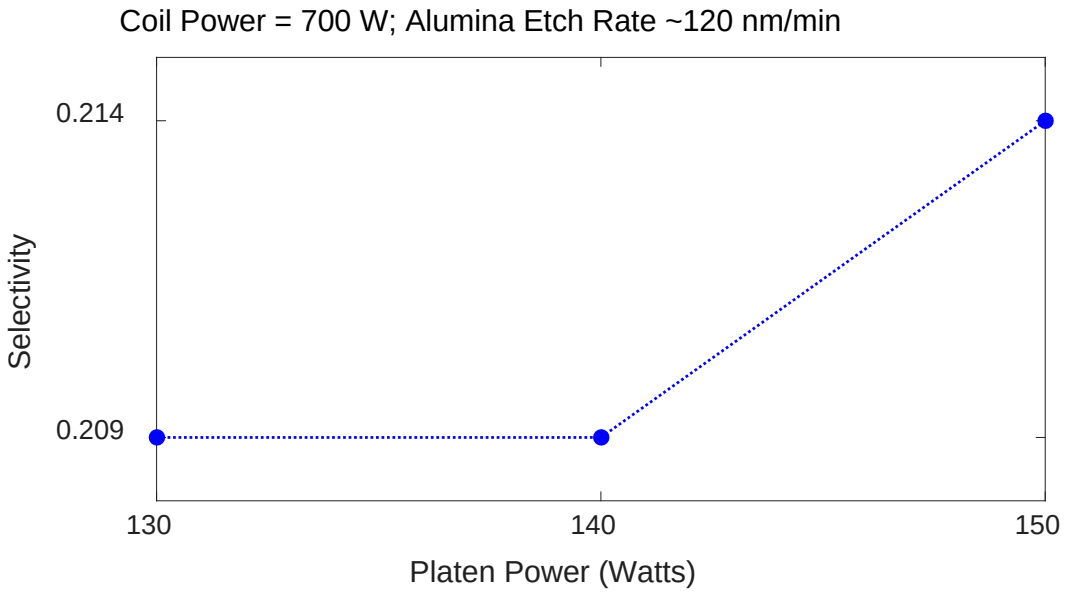

Figure 29 - Selectivity measurement with coil power set to 700 W. Platen power is swept.

The coil power was increased to 800 W. Once again I swept the platen power. So, the chamber pressure was set to 5 mTorr, the coil power to 800 W, and gas flow rates at BCl_3/Cl_2 25/25 sccm. Once again, I measured the etch rate and selectivity with respect to NEB (Figure 30). The etch rate turned out to be around 140 nm/min which is very good for my application. The selectivity is now also acceptable. In the next step, I modified the BCl_3 to Cl_2 ratio in the hope to increase the selectivity even more.

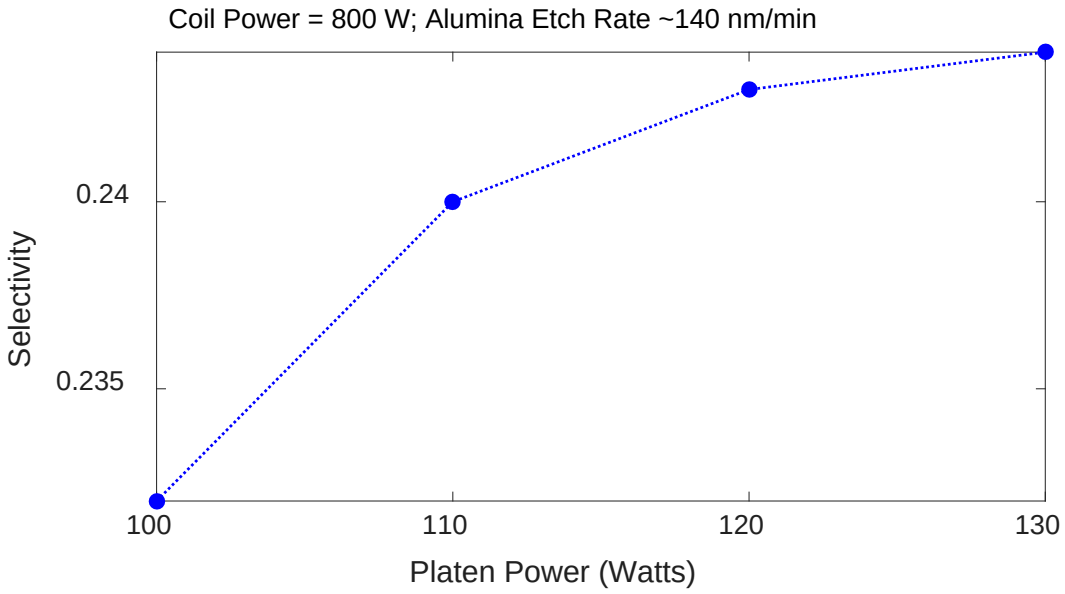

Figure 30 - Selectivity measurement with coil power set to 800 W. Platen power is swept.

After finding a suitable plasma condition in terms of coil power and platen power. I went ahead to optimize the gas ratio. This time I used both NEB and ZEP for selectivity measurements. So, the chamber pressure was set to 5 mTorr, the coil power to 800 W, the platen power to 150 W. I measured selectivity with respect to NEB (Figure 31) and (ZEP Figure 32). It is evident from both figures that the higher the BCl_3 content the higher the selectivity. However, since BCl_3 preferentially removes Oxygen from alumina I have to make sure a higher BCl_3 content would not result in rough sidewalls. That is why I continued with performing XPS measurement to make sure the Oxygen to Al ratio of alumina films before and after exposure to plasma does not change much.

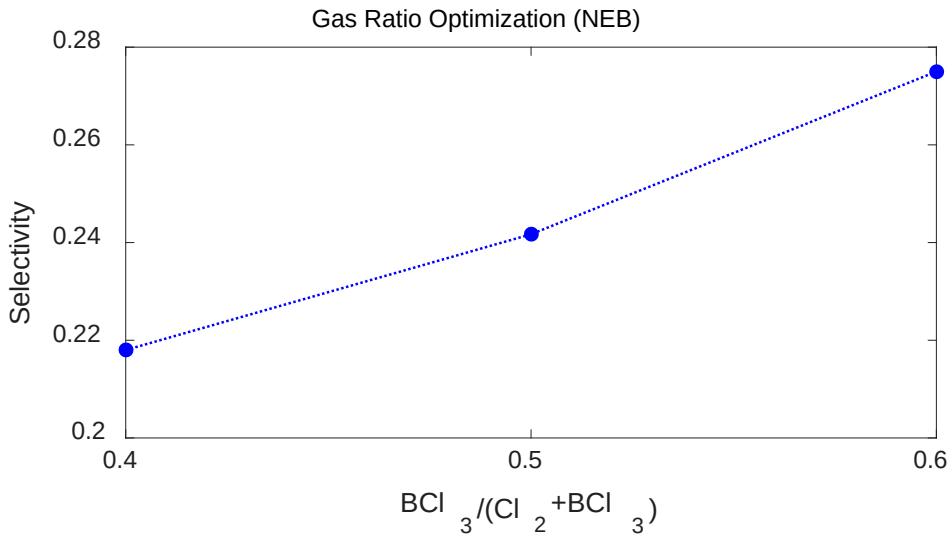

Figure 31 - Selectivity measurement (for NEB) with coil power set to 800 W, platen power set to 150 W. Gas ratio is swept.

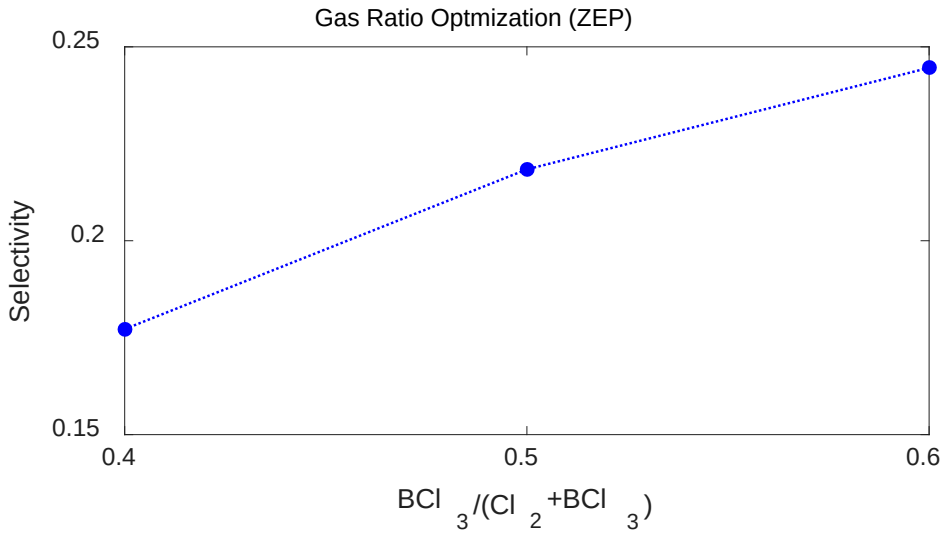

Figure 32 - Selectivity measurement (for ZEP) with coil power set to 800 W, platen power set to 150 W. Gas ratio is swept.

Basically, I prepared three ALD alumina pieces, exposed them to BCl_3/Cl_2 plasma at different gas ratios and measured the Oxygen to Al ratio of the final film. For the pristine as-deposited ALD alumina, the Oxygen to Al ratio turned out to be 1.203. I expected the ratio of the as-deposited film to be 1.5 (three Oxygen atoms per two Al atoms), but this

lower ratio does not come as a big surprise as the as-deposited ALD alumina film is not necessarily stoichiometric Al_2O_3. Anyways, I selected the recipe which provided Oxygen to Al ratio as close to the as-deposited film as possible. The Oxygen to Al ratio of different exposed films turned out to be as follows: For BCl_3/Cl_2 20/30 the ratio was 1.043, for BCl_3/Cl_2 25/25 the ratio was 1.094, and for BCl_3/Cl_2 30/20 the ratio was 1.170. Interestingly, the process which yielded the highest selectivity (BCl_3/Cl_2 30/20), also resulted in the Oxygen to Al ratio closest to the as deposited alumina film. That is why, I finalized my etching recipe as follows: pressure 5 mTorr, coil power to 800 W, platen power 150 W, BCl_3/Cl_2 30/20 sccm.

4.2.2 Sidewalls of SiN Waveguides Etched with Alumina Hard Mask

After finalizing the alumina etching recipe, I continued to pattern some waveguide structures on SiN using alumina as hard mask to examine the quality of my alumina etching process. Basically, I deposited 30 nm ALD alumina on a SiN sample. Then, patterned the waveguides with NEB as mask using EBL, then etched the alumina underneath NEB using the alumina etching process that I have developed in a Plasma-Therm ICP system, then etched the SiN film using patterned alumina as hard mask in an Oxford RIE system. Figure 33 shows the SEM from the etched sidewalls of the SiN film. As we can see, the sidewalls are very smooth, proving the developed alumina etching process works very well without producing excess sidewall roughness.

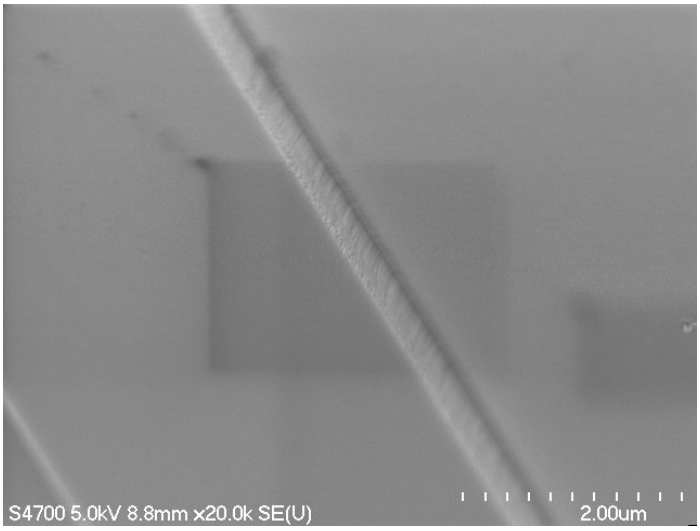

Figure 33 – SEM micrograph of SiN waveguide etched using alumina as hard mask.

4.2.3 Strange Residue on SiN after exposure to Chlorine-based Plasma

Before moving on to the discussion of etching and characterizing optical devices, I should discuss something else. During the alumina etching step, when the whole alumina film is etched and the SiN film gets briefly exposed to plasma some strange residues start to form on the sample. Figure 34 shows the dark field micrograph of the SiN sample with such strange residues formed on it.

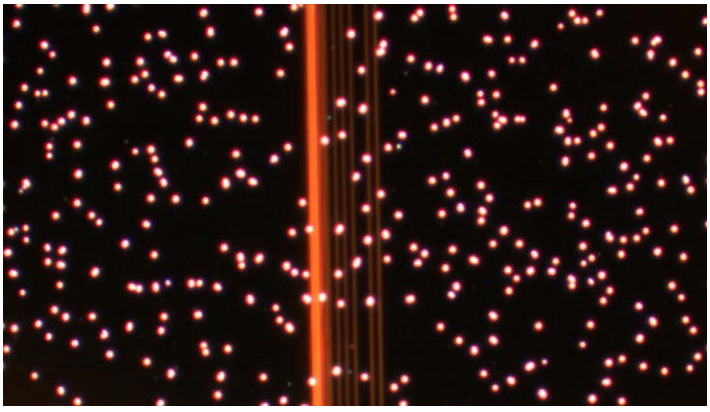

Figure 34 – Strange residues form on SiN sample after exposure to alumina etching process.

These residues seem to be sensitive to light and evolve over time. Figure 35(a) shows a dark field optical micrograph of a SiN sample exposed to the alumina etching plasma (for a few seconds) with the strange residues formed on it. The image is captured right after taking the sample out of the etching system. Figure 35(b) shows dark field optical micrograph of the same SiN sample after 7 minutes. As seen from the images, the shapes and sizes of the residues evolve over time. The growth stops after about 10 minutes. I saw similar residues forming on a bare SiN sample when exposed to Cl_2-only, BCl_3-only plasmas as well. I believe, SiN produces some nonvolatile byproducts as it reacts with Chlorine-containing plasma, which later redeposit on the surface. The residues are easily removed using a brief rinse of with DI water without leaving any marks on the SiN sample.

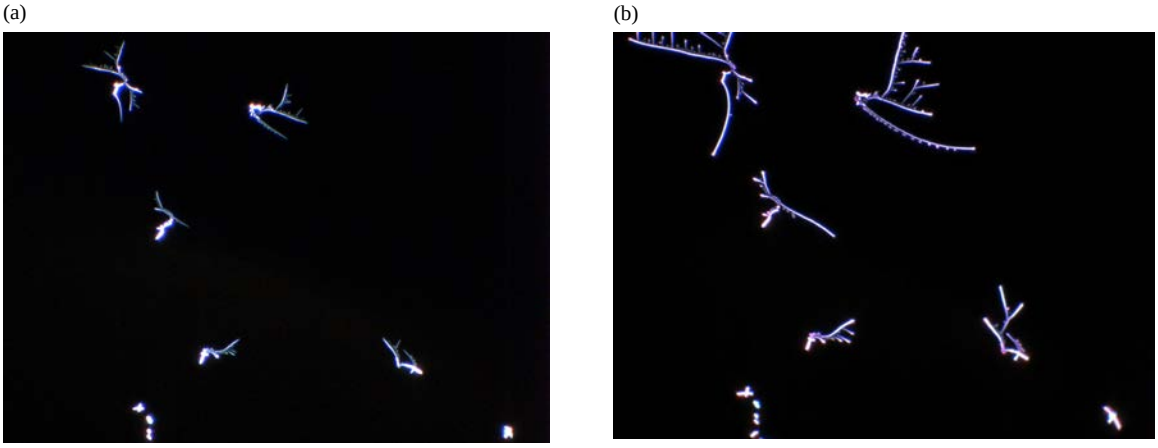

Figure 35 - (a) Residues form on SiN right after removing the sample from etching chamber. (b) The same residues after 7 minutes.

4.2.4 Alumina as Hard Mask to Etch SOI for Devices at 1550 nm Wavelength

As we saw in the previous section, after extensive and careful optimizations, I finalized my ICP etching process on a Plasma-Therm ICP system for alumina as follows: coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm.

Using alumina as hard mask for dry etching the stack of SiN/SiO_2 might lead to the introduction of excess roughness on the sidewalls of waveguides and resonators which may arise from either non-uniform deposition of alumina or the etching process in which alumina is patterned. The best way to test this is to fabricate microring resonators using alumina as mask and measure their Q's. The final application of this process development would be to etch deep profiles in SiN/SiO_2 devices for visible applications. But, as an initial proof of concept, using alumina as hard mask, I fabricated test resonators designed at near 1550 nm wavelength both on SOI and SiN to check how good this process works.

For the case of Si, an SOI piece was coated with 25 nm alumina in an ALD chamber at 250^o C using Trimethylaluminum and H_2O as gas precursors. Each of the precursors were pulsed briefly (60 milliseconds) with 10 second purge time between them. I should note that dirt and other particles on the surface of the wafer (when it goes into the ALD deposition chamber), act as seed layers for ALD deposition, and the thickness of the final layer at those specific sites would end up more than the rest of the sample. These kinds of non-uniformities on the sample would lead to a non-uniform surface after patterning alumina and might get transferred to the final etched layer (Si or SiN). That is why I have to make sure the surface of the SOI pieces are free of particles before placing them inside the ALD chamber. Therefore, before putting the samples inside the ALD chamber, the SOI pieces were thoroughly cleaned in ultra-sonication bath in Acetone, Methanol, and Isopropyl Alcohol, each for at least 10 minutes, respectively.

I then patterned the top alumina using HSQ and e-beam lithography, etched the alumina using the BCl_3/Cl_2 recipe that was developed in an ICP chamber, and finally etched the underneath Si layer using Cl_2 plasma in an ICP chamber. The process parameters for

etching alumina are as follows: coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm. After successful etching of the top alumina layer, the Si layer of the test sample was etched in our standard Si etching process using Cl_2 plasma. The samples were then cleaned in hot Piranha solution to remove the alumina residues before optical characterization.

Ring resonators with 2 μm and 10 μm radii coupled to waveguides were written on the SOI sample to check the optical quality of the overall etching process. Along with the test sample, a control SOI piece was also etched in Cl_2 with only HSQ as the mask to see how the Q of the resonators etched with the alumina as the hard mask compare with the ones fabricated using the control process. To get a fair comparison the HSQ residues on top of the control sample was removed by a quick dip in buffered oxide etchant (BOE).

Figure 36(a) shows a top view SEM image of a 2 μm radius microring on the control sample (HSQ mask). Figure 36(b) shows a 2 μm radius microring on on the test sample (alumina mask). As we can see, the sidewall roughness on both samples are on the same order. Figure 36(c) shows the transmission of a waveguide coupled to a 10 μm radius microring both on the control sample and the test sample. The loaded Q of both microrings are on the same order (40k). This supports the idea that by using alumina as the hard mask no extra roughness are introduced during the etching.

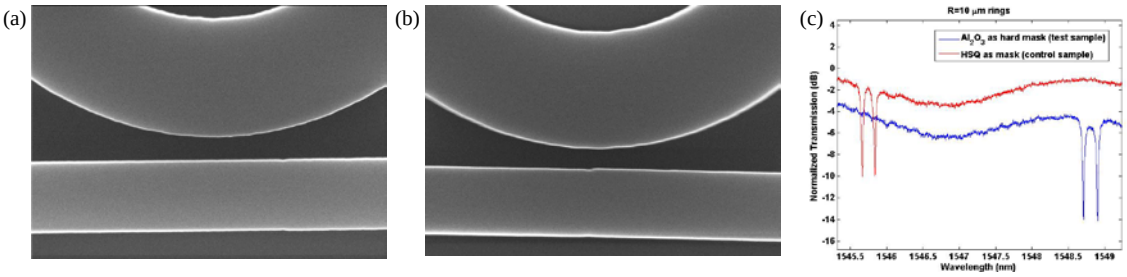

Figure 36 - Top view SEM image of a 2 μm radius multimode microring with (a) HSQ as etching mask (control sample) and (b) alumina as etching mask (test sample). (c) Normalized transmission of a waveguide coupled to a 10 μm radius microring both for a test sample etched using alumina and a control sample etch with HSQ as the mask.

4.2.5 Alumina as Hard Mask to Etch SiN for Devices at 1550 nm Wavelength

For the case of SiN, a SiN (on 4 μm SiO_2) piece was first cleaned in ultrasonic bath similarl to the SOI sample, then coated with 35 nm of alumina in an ALD chamber to act as the hard mask. I then patterned the top alumina using ZEP and e-beam lithography, etched the alumina with the developed etching recipe, and finally etched the underneath SiN layer using Fluorine plasma in an RIE chamber. The process parameters for etching alumina are as follows: coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm. After successful etching of the top alumina layer, the ZEP residues on top of the samples were removed in hot 1165, and then the SiN layers of the test sample was etched in our standard SiN etching process using Fluorine based plasma. The samples were then cleaned in hot Piranha solution to remove the alumina residues before optical characterization.

Ring resonators with 60 um radius coupled to waveguides were written on the SiN sample to check the optical quality of the overall etching process. Along with the test sample, a control SiN piece was also etched with only ZEP as the mask to see how the Q

of the resonators etched with the alumina as the dry mask compare with the ones fabricated using the control process. In order to get a fair comparison the ZEP residues of the control sample were also removed using Piranha solution.

Figure 37(a) shows a top view SEM image of a pattern on the control sample (ZEP mask). Figure 37(b) and Figure 37(c) show a pattern on one the test sample (alumina as mask). As we can see, there are some strange residues left inside the trenches of the alumina sample.

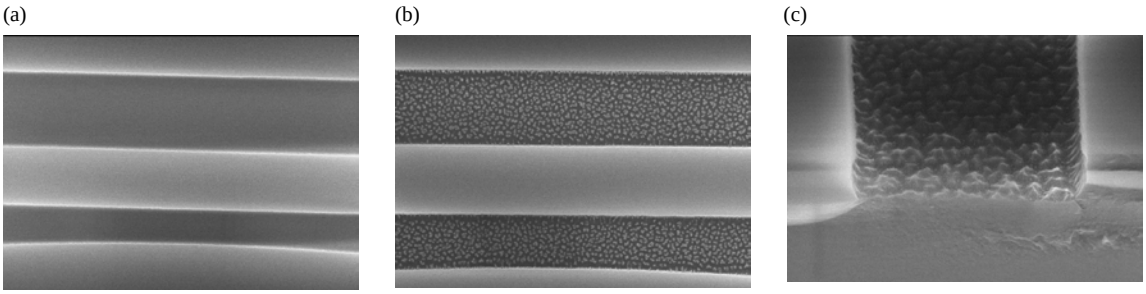

Figure 37 - Top view SEM image of a patterned structure on SiN using (a) ZEP (control sample) and (b) alumina (test sample). (c) Tilted view (45 degrees) SEM image of the cleaved facet of (b).

Up to now, I showed that using alumina to pattern SOI wafers led to similar Q's as compared to the HSQ control sample. However, for the case of patterning SiN using alumina as the hard mask and using ZEP to pattern this hard mask I faced some difficulties in terms of strange residues showing up inside the trenches. As shown in Figure 37, the trenches in the control samples (etched with ZEP) does not have in those residues, unlike the test sample (etched with alumina). I performed a thorough investigation and was able to pin point where those residues came from.

A SiN piece was first thoroughly cleaned in ultrasonic bath in Acetone, Methanol, and Isopropyl Alcohol to get rid of dirt on the sample before going through ALD, each for at least 10 minutes, respectively. After the cleaning step, the sample was transferred to ALD chamber to grow 25 nm alumina to act as hard mask. After the SiN piece was ready for fabrication, I performed step-by-step fabrication and SEM inspection to figure out which step causes those strange residues. I wrote four copies of the optical patterns (microresonators coupled to waveguides), and patterned the top alumina using ZEP and e-beam lithography. I also wrote a control sample (SiN patterned with only ZEP) to compare the Q of my test samples (alumina as hard mask) with it. I then etched the top alumina on all the copies at the same time using my previously developed alumina etching process in an ICP chamber (coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm). I cleaved out one of the copies and inspected the sample by taking SEM images right after the alumina etch step (Figure 38). As we can see from the figure, the top surface of the ZEP becomes porous after the alumina etching step. This by itself is not the source of the problem (since the trenches are still clean and free of strange residues like the ones in Figure 37), and this proves that the residues inside trenches are not caused in the alumina etching step.

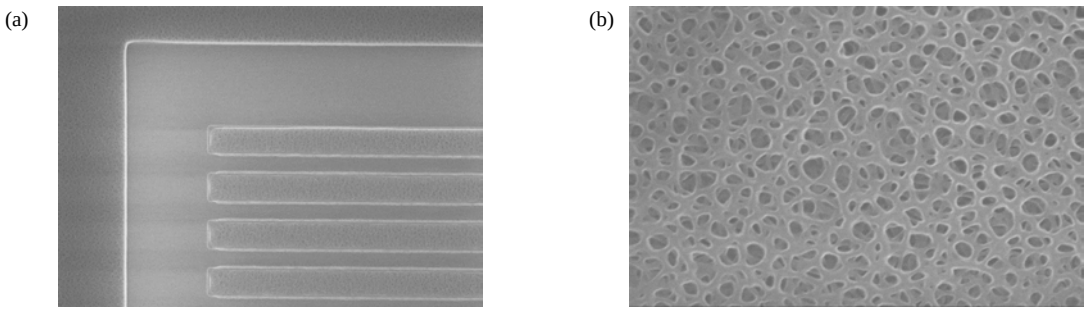

Figure 38 - (a) Top view SEM image of patterned Alumina on SiN using ZEP. (b) Zoomed in SEM of (a).

I then continued the fabrication process on the rest of the copies. The next step was to remove the ZEP residues from the top of the test samples, as I no longer needed them to be there. ZEP is an organic based e-beam resist and is easily removed when exposed to O_2 plasma. I performed 1 min O_2 plasma on the samples, and again cleaved a copy from the chip for SEM inspection (Figure 39).

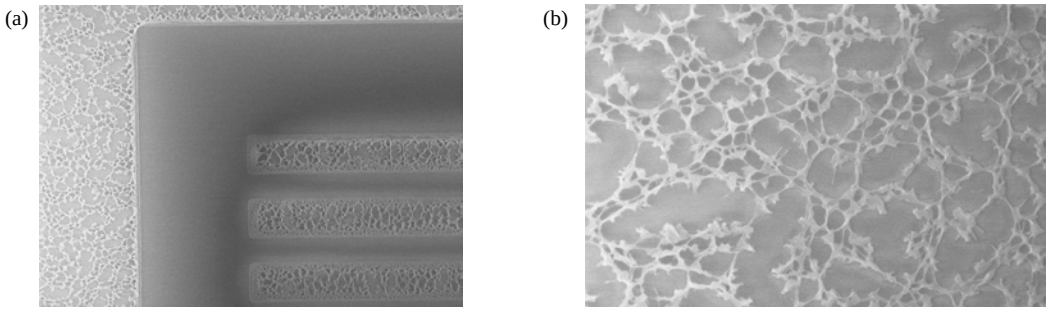

Figure 39 - (a) Top view SEM image of patterned Alumina on SiN after 1 min O_2 plasma to remove the ZEP residues. (b) Zoomed in SEM of (a).

SEM results (Figure 39) show that O_2 had not been able to fully remove ZEP residues from the top of the samples. As I mentioned earlier, ZEP is an organic based e-beam resist and should have been completely removed in O_2 plasma. I even increased the duration of the O_2 plasma to 3 min, and even resorted to using hot 1165 (a harsh organic solvent) to get rid of those residues with no luck. This suggests that during the alumina etching process some inorganic element or elements are incorporated into the ZEP film and had made it irremovable in O_2 plasma and hot 1165. I was later able to remove the ZEP residues using hot Piranha, however, I could not use it on the samples at this stage since Piranha also removes the alumina underneath ZEP which is required to stay there to act as hard mask during the following SiN etching step. I should again add that, the residues from the ZEP left on the sample do not cause any problem by their own, because the strange residues that

we are after, show up inside the trenches not on the SiN layer. So, this proves that the residues inside trenches do not show up after the O_2 plasma step either and that I can continue with etching the SiN layer.

I then continued the fabrication process on the final two copies of my optical patterns. The next step was to etch the SiN layer using alumina as dry mask. I fully etched the SiN layer on one of the copies (400 nm), however I only etched half the SiN layer on the last one (200 nm) to see if the residues inside tranches are on the SiN layer or on the bottom cladding (oxide) layer underneath the SiN film. The fully etched sample was then cleaned using hot Piranha to remove the remaining alumina from the top of the sample to be able to optically characterize the samples as well. Figure 40(a) and Figure 40(b) show SEM images of the half and fully etched copies, respectively. As shown in these SEM images the strange residues show up in both samples. This suggests that the strange residues are etched in the SiN layer and not necessarily on the buried oxide layer.

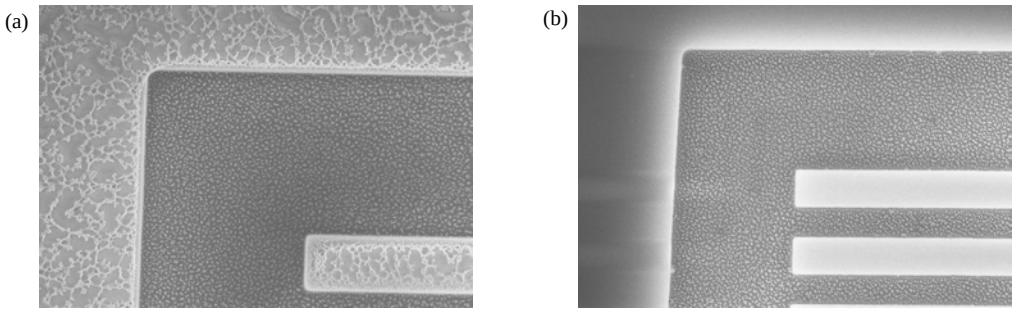

Figure 40 - (a) Top view SEM image of half etched (200 nm) SiN using alumina as dry mask. (b) Top view SEM image of fully etched (400 nm) SiN using alumina as dry mask after Piranha cleaning to remove the remaining alumina.

As shown in Figure 40, unlike for the case of half etched SiN sample, we do not see the ZEP residues outside the trenches on top of the SiN layer for the fully etched sample.

This is due to the fact that the fully etched sample had been cleaned in hot Piranha and, as I mentioned earlier, hot Piranha gets rid of those ZEP residues.

So, the final conclusion of where those strange residues come from is that, during SiN etching in Fluorine-based plasma, the exposed alumina on the bulk of the sample reacts with the plasma and the nonvolatile byproduct (AlF_3) acts as micro-mask inside the trenches and results in non-uniform etching.

After figuring out the source of the problem, I continued with the characterization of the samples (both the test SiN etched using hard mask and the control sample etched with ZEP) to see how much those residues inside the trenches degrade the Q of the microresonators. In order to get a fair comparison, the SiN layer of the test sample and the control sample were etched simultaneously. Ring resonators with 60 um radius coupled to waveguides were written on the samples to check the optical quality of the overall etching process. The remaining ZEP on top of the control sample was also removed using Piranha solution. Figure 41(a) shows the transmission spectrum of a waveguide coupled to a 60 um radius microdisk on the control sample (ZEP as mask). The average loaded Q of the resonances in this transmission is around 1 million. Figure 41(b) shows the transmission spectrum of a waveguide coupled to a 60 um radius microdisk on the test sample (alumina as hard mask). The average loaded Q of the resonances in this transmission is around 500k. This factor of 2 lower Q can be explained by arguing that the interaction of those strange residues inside the trenches with the optical mode inside the resonator, results in optical loss and lower Q's. I should note that this is by no means a show stopper for my proposed etching process, as the problem is caused due to having ZEP (a positive-tone e-beam resist)

as my initial mask to pattern alumina. My final patterns will be etched using HSQ (a negative-tone e-beam resist) as the e-beam resist to pattern the alumina hard mask.

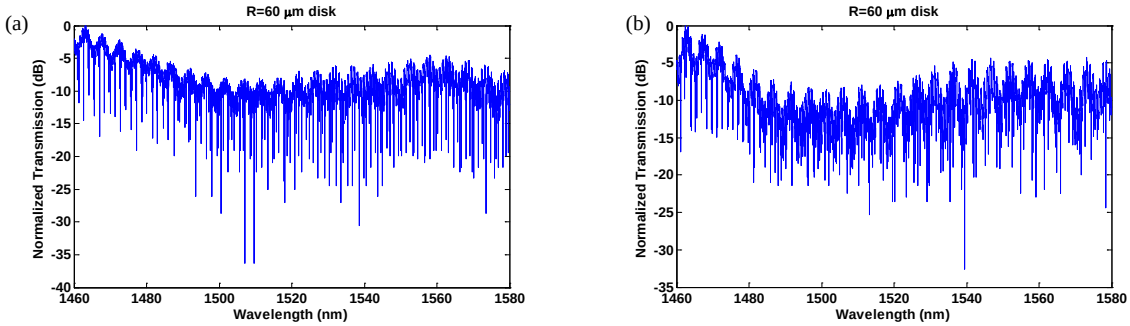

Figure 41 - Normalized transmission of a waveguide coupled to a 60 um radius microdisk for (a) the control sample etched with ZEP as the mask and (b) the test sample etched with Alumina as dry mask.

I should finally add that I tried using short BOE wet etching to try to smooth out the residues inside the tranches in an attempt to increase the Q of the resonators in the test sample. Figure 42(a) shows a cross-sectional SEM image of a sample with SiN non-uniformly etched inside the tranches. Figure 42(b) shows a cross-sectional SEM image of the same sample after putting it in BOE for 1 min. As we can see, the non-uniformities tend to smooth out to some extent after BOE etching, however, an optical characterization of the sample showed that this does not result in Q enhancement of the resonators. This suggests that the non-uniform etching has also caused roughness on the sidewalls and decreased the Q of the resonators on the test sample accordingly.

(a) (b)

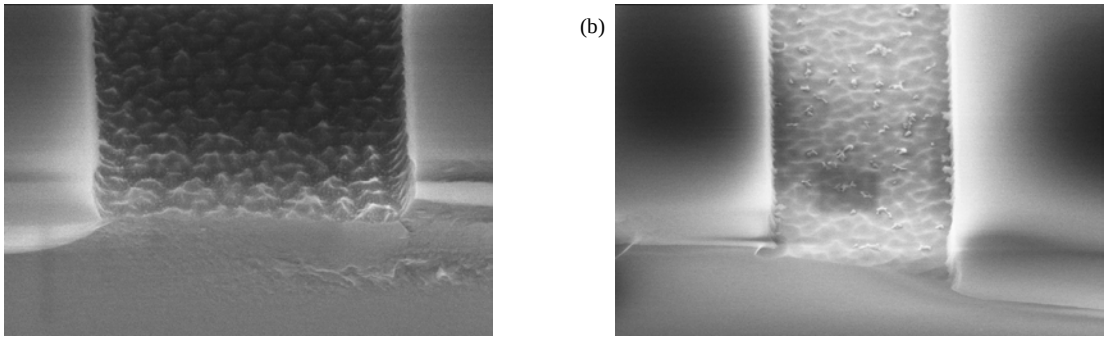

Figure 42 - Cross-sectional SEM image of residues inside the trenches (a) before BOE etch and (b) after immersing the sample for 1 min inside BOE.

4.2.6 Effect of Negative vs. Positive Tone E-beam Resist on Micro-masking

We saw that using ZEP (positive-tome e-beam resist) to pattern the alumina on top of SiN will cause micro-masking and result in a lower Q as compared to the control sample. I also tested HSQ (negative tone e-beam resist) to pattern alumina. I used another SiN piece etched with ZEP as control sample for comparison.

A SiN piece was first thoroughly cleaned in ultrasonic bath in Acetone, Methanol, and Isopropyl Alcohol, each for at least 10 minutes, respectively to remove any particles on the surface of the samples. After the cleaning step, the sample was transferred to ALD chamber to grow 25 nm alumina to act as the hard mask. I wrote optical patterns (microresonators coupled to waveguides), and patterned the top alumina using HSQ and e-beam lithography. I also wrote a control sample (SiN patterned with only ZEP) to compare the Q of my hard mask test samples with it. I then etched the top alumina of the sample using my previously developed alumina etching process in an ICP chamber (coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm). I then continued the fabrication process on the sample. The next step was to etch the SiN layer using alumina as the dry mask. I etched the SiN layer using our standard SiN anisotropic

Fluorine-based etching process. The sample was then cleaned using hot Piranha to remove the remaining alumina from the top of the sample to be able to optically characterize the sample as well. Figure 43(a) and Figure 43(b) show the SEM images of test sample after the final fabrication step. Figure 44(a) and Figure 44(b) show similar SEM images of the control sample (SiN patterned with only ZEP) after removing the remaining ZEP in hot Piranha. As shown by the SEMs, the sidewall roughness on the two samples are on the same order, which again suggest that the alumina etching process does not add excess roughness to the sample.

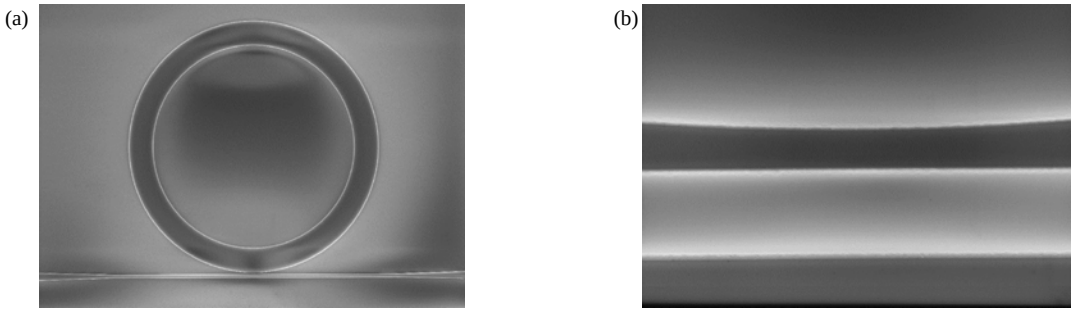

Figure 43 - Top view SEM image of (a) a microresonator coupled to a waveguide etched using alumina as hard mask and HSQ to pattern the alumina and (b) the coupling gap between the microresonator and the waveguide.

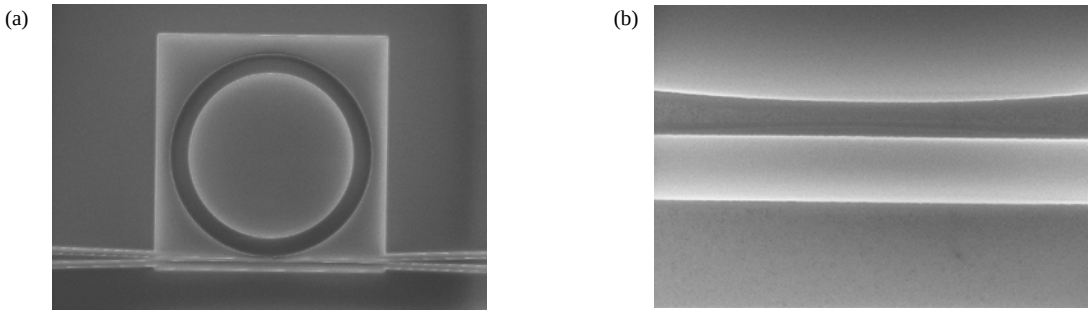

Figure 44 - Top view SEM image of (a) a microresonator coupled to a waveguide etched using ZEP (control sample) and (b) the coupling gap between the microresonator and the waveguide.

I then continued with the characterization of the samples (both the test SiN etched using hard mask and the control sample etched with ZEP) to see how do the Q's of the microresonators compare. In order to get a fair comparison, the SiN layer of the test sample and the control sample were etched simultaneously. Ring resonators with 40 um radius coupled to waveguides were written on the samples to check the optical quality of the overall etching process. The remaining ZEP on top of the control sample was also removed using Piranha solution. Figure 45(a) shows the transmission spectrum of a waveguide coupled to a 40 um radius microring on the control sample. The average loaded Q of the resonances in this transmission is around 1 million. Figure 45(b) shows the transmission spectrum of a waveguide coupled to a 40 um radius microring on the test sample. The average loaded Q of the resonances in this transmission is also around 1 million.

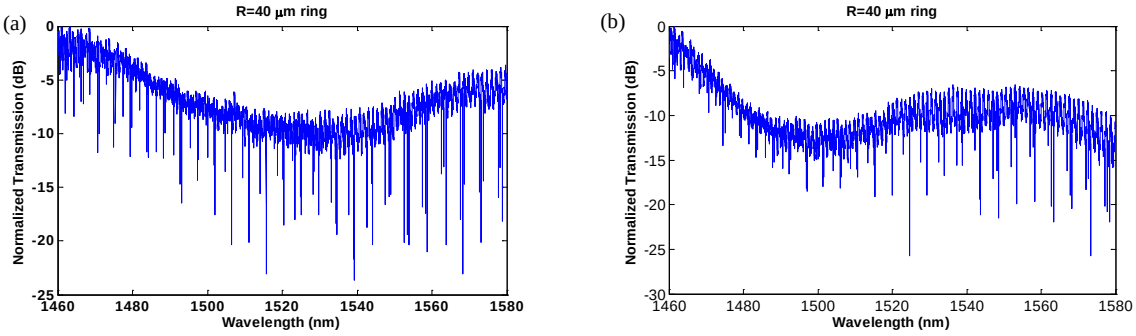

Figure 45 - Normalized transmission of a waveguide coupled to a 40 um radius microring for (a) the control sample etched with ZEP as the mask and the test sample etched with Alumina as the mask.

An interesting point to note here is the fact that as we saw earlier, devices whose alumina were etched with ZEP as mask showed severe micro-masking effect around the resonators. However, devices whose alumina were etched with HSQ as mask showed no such effect. As discussed earlier, I believe the reason has to do with the tone of the e-beam resist (positive vs. negative) being used. For the case of alumina being patterned with ZEP

(positive tone resist), the majority of the surface of the sample will be covered with alumina after the exposed alumina regions are etched in plasma. However, for the case of alumina being patterned with HSQ (negative tone resist), only a fraction of the surface of the sample will be covered with alumina (just the top of waveguide and resonators) after the unexposed alumina regions are etched in plasma. So, when the ZEP-etched sample goes for the SiN etching in the Fluorine-based plasma, the majority of the surface is covered with alumina. The Fluorine-based plasma then reacts with alumina and the byproduct (AlF_3), being a nonvolatile compound, stays inside the etching chamber and acts as micro-mask on the sample. However, the HSQ-etched sample has a very low content of alumina on its surface, and the micro-masking effect does not show up as severely or does not happen at all. I should add that I was later able to get rid of those grassy defects even on the samples which had alumina removed using a positive-tone resist (ZEP or NEB) by reducing the RIE plasma power (during the SiN etching step), whereby reducing the rate of AlF_3 being sputtered away from the surface and redeposited somewhere else to act as micro-mask.

4.2.7 Alumina Etched with HSQ as Hard Mask

Up to now, we saw that using ZEP to pattern and etch the alumina on top of SiN will cause micro-masking and result in a lower Q as compared to the control sample. This is why I chose another e-beam resist, namely, HSQ (a negative tone e-beam resist) to pattern the alumina. Here, the control sample to compare the quality factors is again a ZEP patterned SiN sample.

When writing with e-beam on insulating materials such as my current substrate 400 nm SiN on 4µm SiO_2, charge dissipating agents such as ESPACER 300Z (a conducting

polymer from Showa Denko K.K.) have to be applied on top of the e-beam resist to avoid pattern deformation and field stitching error due to charge-up effect on the sample. ESPACER 300Z is compatible with ZEP and PMMA and perfectly covers the surface of these e-beam resists after the spin coating process. Unfortunately, ESPACER 300Z is incompatible with HSQ e-beam resist. If ESPACER 300Z is applied on HSQ under the standard single-step spin condition of 2500 rpm (with ramp speed of 2500) for 30 seconds, the resulting film will not uniformly cover the surface of the sample, and the EBL process will be imperfect. Figure 46 shows the SEM image of one of the test samples (alumina used as hard mask) after the final SiN etching step. As we can see the microring (left arm in the SEM) suffers from severe sub-field stitching error. This shows that the standard spin coating process of ESPACER 300Z on HSQ did not result in good surface coverage, and the sample was not protected against charge accumulation in the EBL writing step. This issue was tackled through modifying the spin coating process of ESPACER 300Z on HSQ to maximize the surface coverage to reduce charge accumulation-related errors in the EBL process. After drop casting ESPACER 300Z on the HSQ-coated sample, it has to be first spun at a lower speed (500 rpm) for 10 seconds, then at a higher speed (2000 rpm) for another 30 seconds. This guarantees that a uniform layer of ESPACER 300Z will cover the whole surface of the sample after the spin coating step.

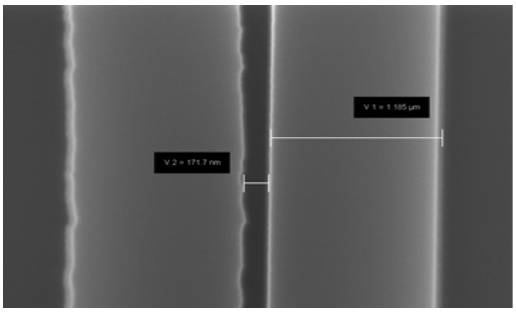

Figure 46 - Top SEM image of a SiN waveguide coupled to a SiN microring after etching, which shows severe field stitching errors on the sidewalls of the microring.

Before moving on to etching the final samples, as a final test, I etched a few SiN devices designed at 1550nm wavelength using HSQ as e-beam resist to pattern alumina. In contrast to the previous patterns, this time I used single mode SiN rings (as opposed to multimode microrings) so that the effect of sidewall roughness is more pronounced on the Q of the resonators, so that the quality of the etching process can be better judged through Q measurement.

So, another SiN on oxide piece was thoroughly cleaned in ultrasonic bath in Acetone, Methanol, and Isopropyl Alcohol. Then 35 nm alumina was deposited on the sample in an ALD chamber. The HSQ was spun on the test sample, and ESPACER 300Z was spun on the HSQ layer using the optimized process. I also prepared a control sample (SiN patterned with only ZEP) to compare the Q of my hard mask test samples with it. I then wrote optical patterns (microrings coupled to waveguides) on both test and control samples using EBL process. Microrings with 1.3 μm width were used instead of wider microrings, because the effect of sidewall roughness is more pronounced for the case of single-mode microrings and we can more efficiently compare the devices on the test sample and the control sample. I then etched the top alumina of the samples using the previously

developed alumina etching processes in an ICP chamber. Then the test samples along with the ZEP-written control sample were etched in an RIE chamber to pattern the SiN layer. The etched devices (control sample and the sample etched with alumina as the hard mask) were then characterized. Figure 47(a) and Figure 47(b) show the SEM image of one of the test samples (alumina used as hard mask) and the ZEP-written control sample after the final SiN etching step. Figure 47(c) and Figure 47(d) show the transmission spectrum of the samples after optical characterization. Average intrinsic Q of the alumina-etched test microrings are around 500k which is higher than the average Q of the control ZEP-written microrings by around 100k. The SEMs along with the characterization results clearly show that alumina can be used as a hard mask to etch good quality structures in SiN, and also proves that not only the alumina etching process does not degrade the Q's of the devices, it also improves them.

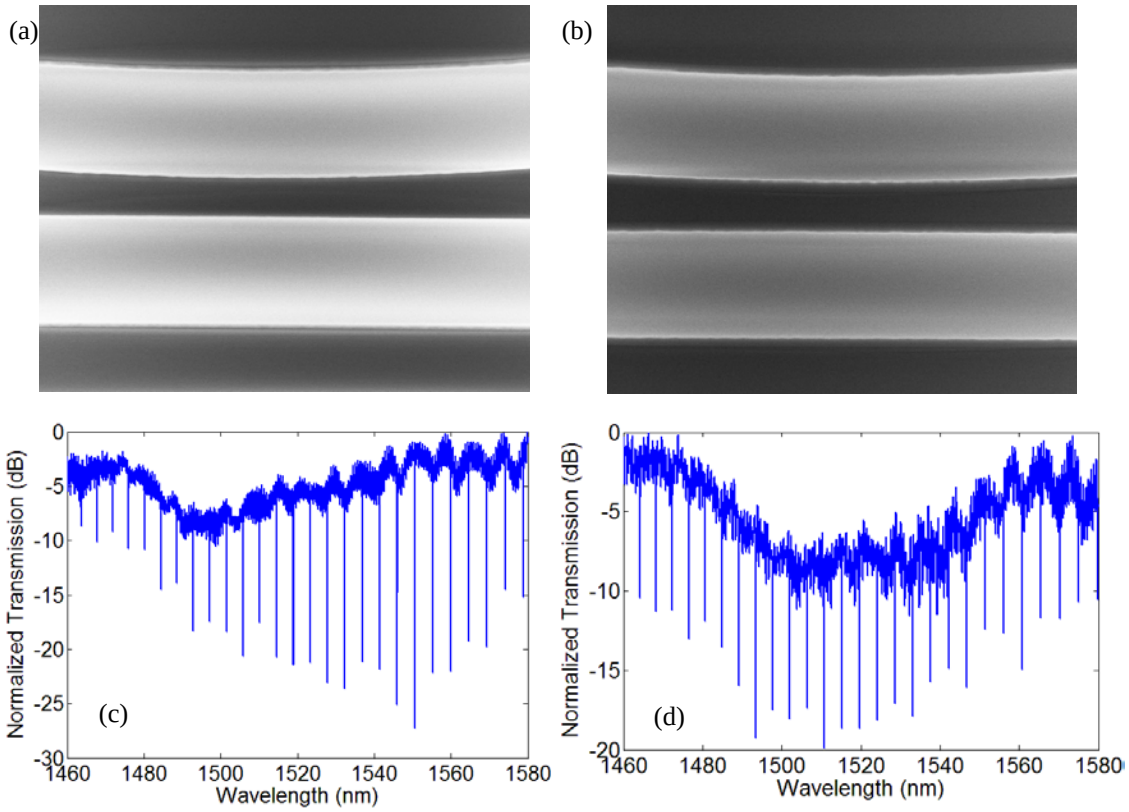

Figure 47 - SEM image of the coupling region between a 40 μm radius microring and a 1.3 um wide waveguide for (a) SiN etched with alumina as the hard mask and (b) SiN etched with ZEP as the mask. (c) Through port response of the structures in (a) and (b) for SiN etched Alumina hard mask (c) and ZEP (d).

4.3 Experimental Results

So far, the alumina etching recipe was developed and optimized. It was also tested to etch different devices in SOI and SiN at 1550 nm wavelength to confirm how good it works through Q measurement. Devices fabricated using alumina as hard mask showed Q's on the same range or even better than those etched using conventional e-beam resists. We now move on to etch ultra-compact high-Q SiN microrings using alumina as hard mask.

High quality stoichiometric LPCVD SiN was deposited on oxide wafers with 4 μm thermally grown SiO2 (as bottom cladding). Then, 30 nm to 60 nm alumina (depending on the final etching depth) was deposited on the wafers in an ALD chamber using Trimethylaluminum (TMA) and H_2O as gaseous precursors at 250º C. Next, ultra-compact resonators with different radii were patterned on each of the substrates using e-beam lithography (EBL) with HSQ as mask. Then, using the developed alumina etching process, the ALD-deposited-alumina films were etched in a Plasma-Therm ICP system to transfer the EBL pattern to the alumina films. Then, the SiN and SiO_2 layers were etched in an Oxford RIE system using anisotropic SiN and SiO_2 etching recipes, respectively.

The SiN film is fully etched and, the bottom oxide cladding is etched at two different depths, 100 nm and 200 nm, to compare the intrinsic Q of the two cases. The parameters for the SiN anisotropic etching process are as follows: chamber pressure 55 mTorr, RF power 175 W, CHF_3:O_2 50:5 sccm. The parameters for the SiO_2 anisotropic etching process

are as follows: chamber pressure 33 mTorr, RF power 200 W, CHF_3:Ar 25:25 sccm. Both of these processes are fluorine-based, meaning that only a very thin film of alumina is enough to etch the whole SiN/SiO_2 stack. After successful etching, the alumina residue is removed from the microdisks and waveguides by cleaning the sample in Piranha solution at 120º C. Figure 48(a) and Figure 48(b) show the top-view SEM image of a 2.5 µm radius SiN microdisk resonator coupled to a waveguide and a focusing grating coupler [129] used to characterize the devices, respectively. The SiN thickness is 400 nm and the bottom oxide is over-etched 200 nm.

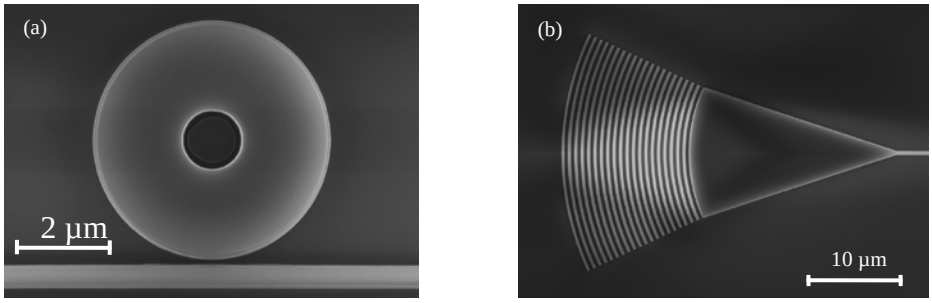

Figure 48 - The top-view SEM image of (a) a 2.5 µm radius SiN microdisk resonator coupled to a waveguide, and a SiN focusing grating coupler. The SiN thickness is 400 nm and the bottom oxide is over-etched 200 nm.

I fabricated ultra-compact microdisk resonators with radii as low as 2.5 µm on SiN/SiO_2 substrates with different SiN film thickness. The fabricated resonators were then characterized by measuring the transmission spectra of the waveguides using a swept-wavelength optical characterization setup near 772 nm. Focusing grating couplers (as shown in Figure 48(b)) were used to couple light into and out of each waveguide. A fiber polarization controller was used to adjust the input polarization to the devices. The output light is detected using a photo-detector and sent to computer through a data acquisition card.

Figure 49(a) shows the TE resonance of a 2.5 µm radius microdisk resonator with an intrinsic Q (Qi) of 60k and an FSR of about 20 nm. The thickness of the SiN film is 400 nm and the bottom oxide cladding is etched by 100 nm. Figure 49(b) shows the TE resonance of a similar 2.5 µm radius microdisk resonator with an intrinsic Q of 140k. The only difference between the two figures is that the bottom oxide cladding in (b) is etched by 200 nm. As expected the extra 100 nm of SiO_2 removal has resulted in increasing the intrinsic Q of the microdisk resonator.

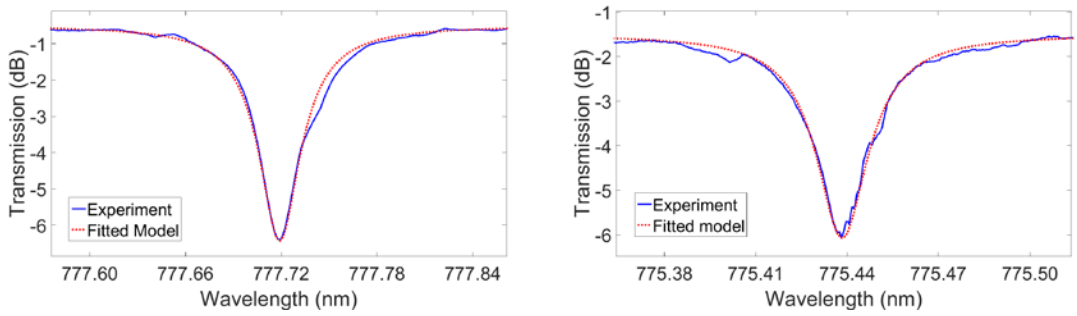

Figure 49 - (a) Transmission spectrum of (a) a 2.5 µm radius microdisk resonator with Qi of 60k, (b) and another 2.5 µm radius microdisk resonator with Qi of 140k. The SiN thickness in (a) and (b) is 400 nm. The bottom oxide cladding is over-etch by 100 nm in (a) and 200 nm in (b). Dashed curves shows a Lorentzian resonance fitted to the experimental data.

Figure 50(a) shows the TE resonance of a 3 µm radius microdisk resonator with an intrinsic Q (Qi) of 98k and an FSR of about 16 nm. The thickness of the SiN film is 300 nm and the bottom oxide cladding is etched by 100 nm. Figure 50(b) shows the TE resonance of a similar 3 µm radius microdisk resonator with an intrinsic Q of 177k. The only difference between the two figures is that the bottom oxide cladding in (b) is etched by 200 nm.

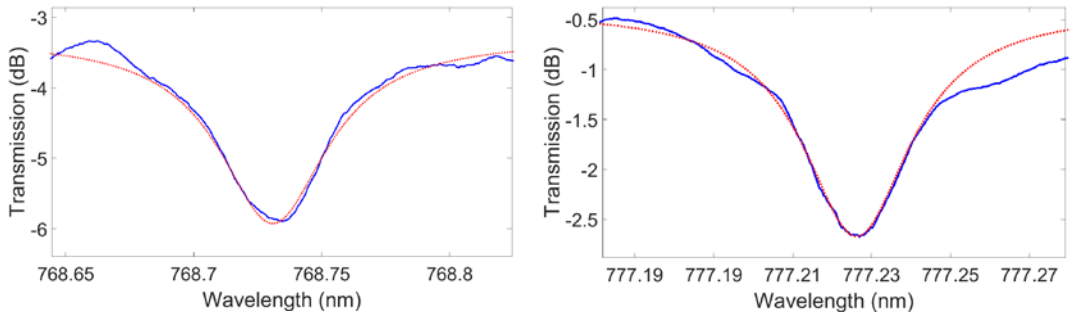

Figure 50 - (a) Transmission spectrum of (a) a 3 µm radius microdisk resonator with Qi of 98k, (b) and another 3 µm radius microdisk resonator with Qi of 177k. The SiN thickness in (a) and (b) is 300 nm. The bottom oxide cladding is over-etch by 100 nm in (a) and 200 nm in (b). Dashed curves shows a Lorentzian resonance fitted to the experimental data.

In summary, a robust etching process to etch deep profiles in SiN/SiO_2 using alumina as hard mask has been developed and carefully optimized. The etching process has been tested on several devices with promising results. Using the developed etching process, ultra-compact microdisk resonators in SiN with large FSRs were fabricated and shown to have very high Q's. The Q's reported here (140k for 2.5µm radius on 400 nm SiN and 177k for 3µm radius on 300 nm SiN) are the highest reported Q's for ultra-compact microring resonators on SiN platform to-date. The developed etching process is not limited to the current application. It could potentially be used to etch different materials up to several microns with perfect sidewalls, where conventional e-beam resists such as ZEP, HSQ, and Ma-N do not provide the required etch resistance. One application would be to etch deep profiles in thick SiN films for dispersion engineering to enable nonlinear effects such as frequency comb generation.

CHAPTER 5. HYBRID GRAPHENE-SIN PLATFORM

5.1 Introduction

As discussed in section 1.2.2, I propose to use the strong free-carrier plasma dispersion effect and ultra-high charge mobility in a hybrid material platform formed by integrating two layers of graphene films on SiN to add tuning capability to SiN. The strong free-carrier plasma dispersion effect in graphene enables ultralow-power modulation of the effective refractive index of waveguides and resonators in the proposed material platform. Figure 51 shows the schematic of the proposed hybrid graphene-SiN platform in which two graphene layers are separated by a thin oxide layer to form a capacitor. The device is a microdisk optical resonator with whispering gallery modes. Free carriers can be accumulated on the two sides of this capacitor (by applying voltage) to change the absorption of graphene and index of refraction based on the free-carrier dispersion effect. This index or absorption change results in changing the resonance wavelength or its extinction. Thus, the transmitted optical power through the waveguide is modulated by the application of the voltage.

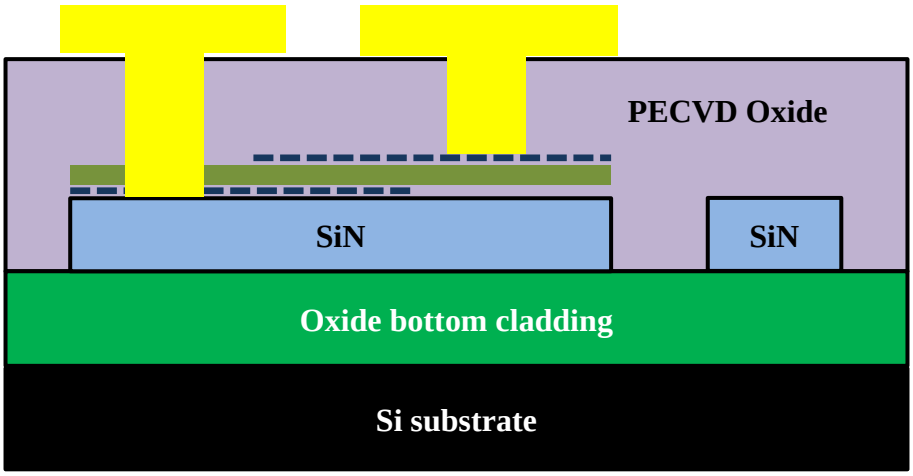

Figure 51 - Schematic of the Graphene-SiN hybrid platform.

The main optical devices that is used here to implement the modulation scheme on are microdisk and microring resonators (shown in Figure 52(a) and Figure 52(b), respectively). Microdisk and microring resonators are both subsections of traveling-wave resonators (TWRs). In TWRs optical field travels around the resonator. If the field interferes constructively with itself after one roundtrip, the resonance condition is satisfied and energy is built up inside the resonator. In microdisk resonators the resonant mode "sees" or interacts with only one etched sidewall, and therefore roughness on the sidewalls play a smaller role in the overall Q of the resonators. Such resonators are commonly referred to as "whispering-gallery mode" (WGM) resonators. The WGM effect is present as long as the inner sidewall of the resonator is far enough not to interact with the optical mode. Microring resonators are designed to support only one mode, and that resonant mode "sees" or interacts with both etched sidewalls, and therefore roughness on the sidewalls play a bigger role in the overall Q of the resonators. Because of this microring resonators tend to have lower Q's than micrdisk resonators.

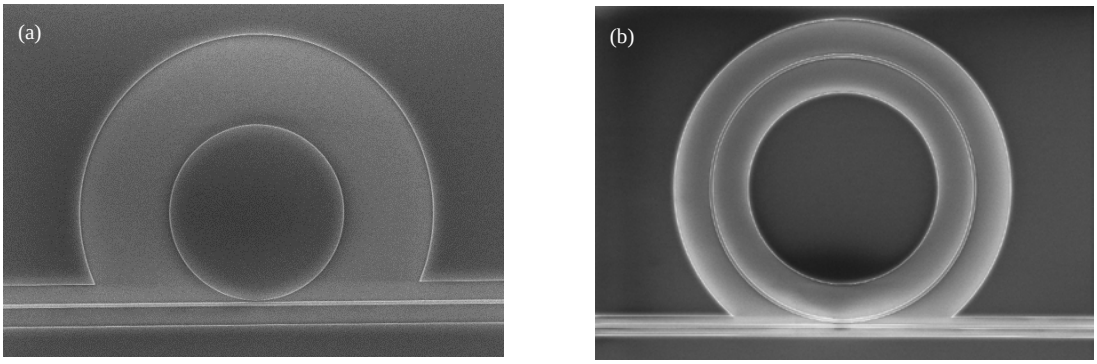

Figure 52 – Top view SEM image of (a) microdisk resonator, and (b) a microring resonator.

5.2 First Fabrication Trial

Here, I present, in detail, the process for forming double-layer graphene devices on SiN, which is very complicated and requires many fabrication steps. In the double-layer graphene structure, the two graphene layers are separated by a thin oxide layer to form a capacitor in which the application of a voltage between the two graphene layers results in charge accumulation in these layers. When this capacitive structure is integrated with a (passive) SiN or Si resonator, the change in the index of refraction of graphene or its absorption results in a change in the resonance wavelength or extinction. Thus, the transmission through the waveguide can be modulated (or switched on and off) by applying a voltage to the double-layer graphene structure.

Our device fabrication process starts with design, optimization, and fabrication of the underlying passive SiN structure, which in the simplest form includes a waveguide coupled to a microdisk/microring resonator. In this work, the properties of the double-layer graphene structure is considered in designing the passive device and optimized using an in-house code implemented in the COMSOL environment. The most challenging part of

the fabrication process was to develop and optimize a reliable transfer process for the two graphene layers. With extensive efforts, this process was optimized, and it can now be used repeatedly with high yield.

5.2.1 Fabrication of Photonic Structures on SiN Substrate

The bottom cladding of my SiN devices is a thick (>3 μm) SiO_2. In order to get minimum scattering from the bottom cladding, I choose high quality thermal oxide. So, the first step of fabrication is to grow thick oxides on prime silicon wafers. This thick oxide layer will prevent the optical modes from leaking into the substrate (Si). As the dry oxidation rate is very low, the majority of the oxidation process is done via wet oxidation. I either grow the oxide in-house at Georgia Tech cleanroom (at 1100° C for over 30 hours) or purchase Si prime wafers with the thermal oxide already grown on them. The next step would be to deposit high quality stoichiometric LPCVD SiN films on the oxidized wafers. I use LPCVD instead of PECVD to end up with devices with lower optical loss.

As discussed in chapter 4, a 400 nm thick SiN results in high effective indicex and allows for dense integration of integrated photonics devices. So, 400 nm LPCVD SiN is grown in-house on the oxide wafers at 800° C. I use dichlorosilane (SiH_2Cl_2, or DCS) and ammonia (NH_3) as source gases. The parameters for the stoichiometric LPCVD deposition on a Tystar furnace at Georgia Tech cleanroom are as follows: pressure 165 mTorr, DCS 50 sccm, NH_3 140 sccm, temperature 800° C. This process deposits SiN at a rate of ~4.4 nm/min. After the LPCVD deposition the wafer is cleaved into chips with suitable dimensions before moving on to the next fabrication steps.

After preparing the substrate (SiN on SiO_2) and cleaving it the photonic structures are patterned. I use e-beam lithography (EBL) since the minimum features of my structures are well in the sub-micron region. For the first round of devices, ZEP (ZEP520A by Zeon cooperation) was used as the e-beam resist. ZEP is a positive-tone resist (resist becomes soluble in developer after being exposed to e-beam) and in order to save on EBL write time only the periphery of the devices is written with e-beam to confine light inside the unexposed regions. ZEP is coated on the substrate and it is spun at 1000 rpm (with ramp speed of 500) for 60 seconds, then baked on a hotplate for 2 minutes at 180° C. After the bake step, there is usually around 750 nm ZEP on the sample. After the bake step the resist-covered SiN substrate is patterned using a JEOL JBX-9300FS EBL system. When writing with e-beam on insulating materials such as my current substrate (400 nm SiN on 4µm SiO_2), charge dissipating agents such as ESPACER 300Z (a conducting polymer from Showa Denko K.K.) have to be applied on top of the e-beam resist to avoid pattern deformations and field stitching error due to charge-up effect on the sample. So, after baking ZEP, and before moving on with the EBL process, I spin coat ESPACER 300Z at 2500 rpm (with ramp speed of 2500) for 30 seconds on the sample. ESPACER 300Z is water soluble and will be easily removed right after the EBL step (before developing ZEP) by rinsing it with DI water for just a few seconds. As will be discussed later, for the final round of a devices ZEP was not used as the e-beam resist, and a modified fabrication process based on the alumina hard mask (chapter 4) was used.

Next, the pattern is transferred to the SiN layer using reactive ion etching (RIE) in an Oxford RIE system with a CHF_3/O_2 gas mixture. The etching parameters are as follows: pressure 55 mTorr, RF power 175 W, CHF_3 50 sccm, and O_2 5 sccm. The etch rate of SiN

and ZEP in this process are around 60 nm/min and 56 nm/min, respectively. So with the selectivity of a little bit over than 1, 400 nm of SiN is easily etched with 750 nm ZEP as mask. Usually a 10-20% extra time is added to the etching step to make sure all the tight openings (for example waveguide-resonator gaps) are fully etched. Integrated photonic devices such are microdisk and microring resonators with different radii coupled to bus waveguides are fabricated. Input and output grating couplers are used to couple light into and out of bus waveguides. The advantage of using grating couplers is that devices can be optically characterized after each step of fabrication to make sure everything has gone according to plan. Figure 53 shows SEM images of one of the fabricated microdisk resonators, and also SEM of an input grating coupler fabricated on the SiN platform.

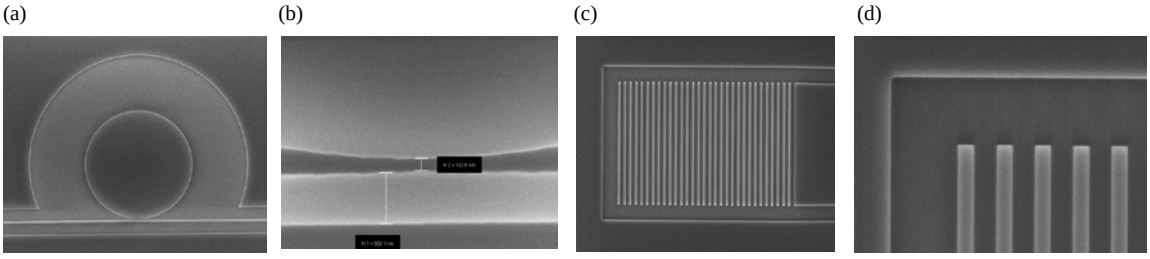

Figure 53 - (a) top-view SEM image of a microdisk resonator fabricated on SiN substrate, (b) zoomed-in SEM image of the gap between the bus waveguide and the microdisk resonator, (c) top-view SEM image of a grating coupler, and (d) zoomed-in SEM of the grating coupler.

5.2.2 Graphene Transfer Process

After discussing the fabrication process of passive SiN devices, here I present the process of transferring graphene to a desired substrate. The graphene I use for my devices is grown using the Chemical Vapor Deposition (CVD) technique on a thin Copper (Cu) film. We do not grow graphene in-house and purchase high quality and mostly single-layer

graphene from ACS material. Figure 54 shows an image of a typical single-layer graphene on Copper foil purchased from ACS material.

Figure 54 - CVD-grown graphene on Copper foil purchased from ACS material

Depending on the size of the chip onto which I want to transfer graphene, I cut the graphene-on-Copper foil into appropriate pieces using sharp razor blades or scissors. I then follow a similar wet transfer process as discussed in [130]. If not performed carefully, the graphene transfer process will not be very successful. Figure 55 shows the SEM from a sample after unsuccessful graphene transfer. As we can see, the graphene is torn in different places. This is not acceptable for my application. Therefore, I had to carefully optimize the transfer process through several test steps.

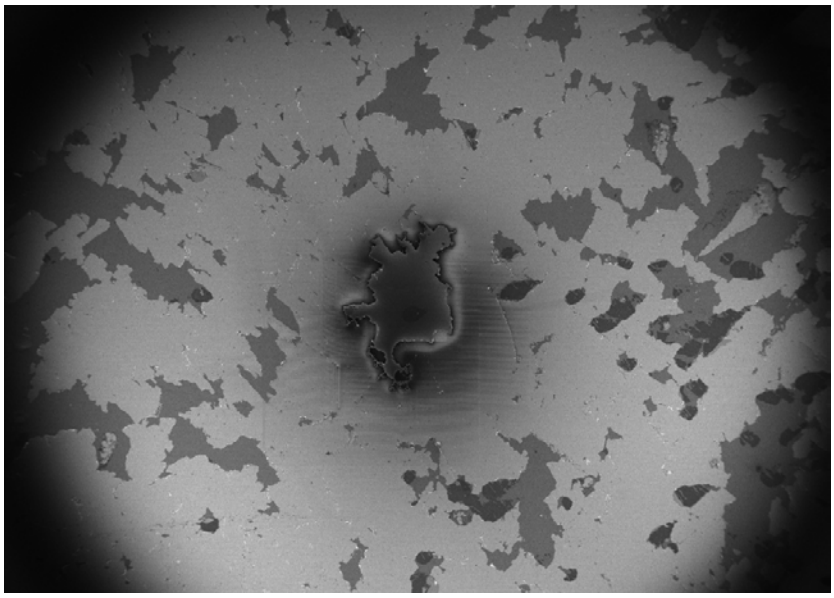

Figure 55 – SEM of a sample with failed graphene transfer process.

After cutting graphene/Cu into an appropriate size, we need to get rid of the Copper and etch it away before transferring graphene on the SiN substrate. To do so, we first need to cover the graphene with a protective layer that is hydrophobic to avoid graphene from sinking in the Copper etching solution after the Copper is completely gone. I use PMMA for this task, and it is spun on the graphene/Cu foil. PMMA will provide mechanical support for the graphene layer after the Cu is etched away. As I mentioned earlier, the Cu foil is very thin; therefore, I need to tape the foil down to a clean glass slide to help with the spin coating process. So, I first place graphene/Cu foil between two clean glass slides and press the slides together to completely flatten out the foil. Then, I tape the foil down on a clean glass slide using Kapton tape on the sides. Using the flat head of a tweezer, I press the tape hard to prevent PMMA going under the gap between graphene/Cu and the glass slide. I then take the sample and spin coat A6 PMMA (from Microchem) on it to get

a ~500 nm thick film. I leave the sample for several hours (or overnight) for the PMMA solvent (here anisole) to evaporate.

During the CVD process, graphene is grown on both sides of the Cu film. But, we only need graphene on one side; therefore, I need to remove graphene from the back side of the foil. After the PMMA is dried out, I carefully remove the tape from the sides of the PMMA/graphene/Cu to avoid causing any wrinkles to the film. I then flip it over and put it on a clean glass slide and press it down with another clean slide to make it flat, tape the sides with Kapton tape once more and etch the graphene on the backside using O_2 plasma in an RIE etching machine. The tapes need to be fully pressed over the sides of the graphene to avoid exposing the PMMA-covered side to O_2 plasma.

The PMMA/graphene/Cu is now ready to be transferred to a wet etching solution to remove the Cu. Several different etchants can be used to remove Cu. Here I use Copper Sulfate. The solution is made by adding DI water and HCl to $CuSO_4$ crystals. After preparing the etching solution I remove the Kapton tape from the sides of the film and place it in the etching bath (Copper side down). Due to the hydrophobic nature of PMMA, the sample floats on top of the solution, and Cu gets etched away. After more than 5 hours that Cu is completely etched, I carefully transfer the sample from the etching solution into DI water and change the DI water several times to remove any Cu or acid residues. I use a concave watch glass for transferring graphene from the acid bath to DI water baths, so that the liquid puddle that forms inside the watch glass protects the PMMA/graphene layer from damage during each transfer. Before the Cu is etched, it provides mechanical support for the PMMA/graphene layer. But after it is etched away the thin PMMA/graphene film needs

to be handled/carried very carefully from one solution to the other to avoid any tears in the film.

After several steps of DI water cleaning the PMMA/graphene film is ready to be transferred to the desired substrate/chip. As the film floats on the DI water I immerse the chip in the DI water and fish the PMMA/graphene out, and let the DI water to dry out for several minutes. I then place the chip on a hotplate to anneal the PMMA/graphene to get rid of any wrinkles on the sample and enhance the adhesion between graphene and the SiN substrate. I increase the hotplate temperature from 40º C to 220 ºC at the rate of 10º C per minute. Then, leave it at 220 ºC for 5 minutes. Then, remove the substrate from the hotplate and allow it to cool down for several minutes.

The next step would be to get rid of the PMMA as we no longer need it. People usually immerse the sample in an Acetone bath for a few hours to remove the PMMA. However, the wet removal of PMMA in Acetone is not very safe, and I noticed that on several samples the graphene layer gets badly torn after this step. Figure 56 shows the SEM of a microring resonator with graphene transferred on it. The PMMA on the graphene was removed by keeping the sample inside Acetone for 2 hours. As we can see, the graphene layer is torn on different parts of the sample. Therefore, I modified the process and used Acetone vapor instead to remove PMMA. Basically, the sample is fixed right above the surface of Acetone. The beaker holding the Acetone is placed on a hotplate at 90º C to increase the rate of evaporation of Acetone. PMMA gets removed from the top surface in a couple of hours, and only graphene is left on the sample. This method (vapor Acetone for PMMA removal) has proved to yield excellent results with minimal damage to graphene.

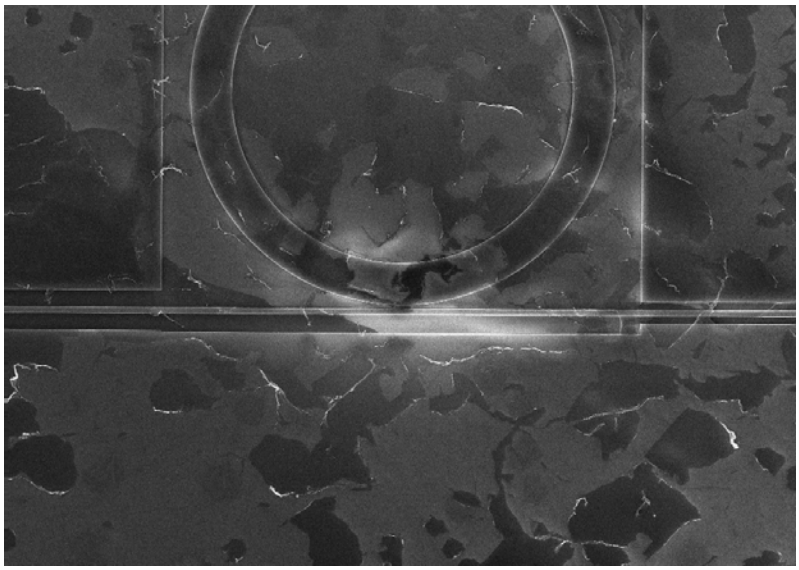

Figure 56 – Failed graphene transfer process on SiN a microring resonator. Sample failed due to the damage to the graphene layer during PMMA removal in Acetone bath.

5.2.3 Transferring Bottom-layer Graphene on Photonic Structures

Now that we became familiar with the graphene transfer process in general, I move on to the discussion of successful transfer of graphene on SiN integrated photonic structures. After fabricating passive devices on SiN, I need to transfer the first layer of graphene (bottom-layer-graphene) on top of the chip. This graphene layer serves as the bottom plate of the capacitor to be formed on top of the devices. In transferring graphene on silicon-on-insulator (SOI) substrates, it is required to first deposit a dielectric layer on top of the Si (i.e., between Si and graphene) to avoid current flowing from graphene to Si layer, whereby shorting the capacitor. This extra step is not required for SiN-based structures due to the insulating nature of SiN. Thus, in my process, the bottom layer graphene layer can be transferred directly on top of the SiN layer. This transfer is performed using the process discussed in the previous section. Figure 57 shows a top view SEM image

of the bottom-layer graphene transferred on a SiN microdisk resonator. As discussed before, the thickness of the SiN layer in this work is 400 nm, which is needed for designing high-Q devices.

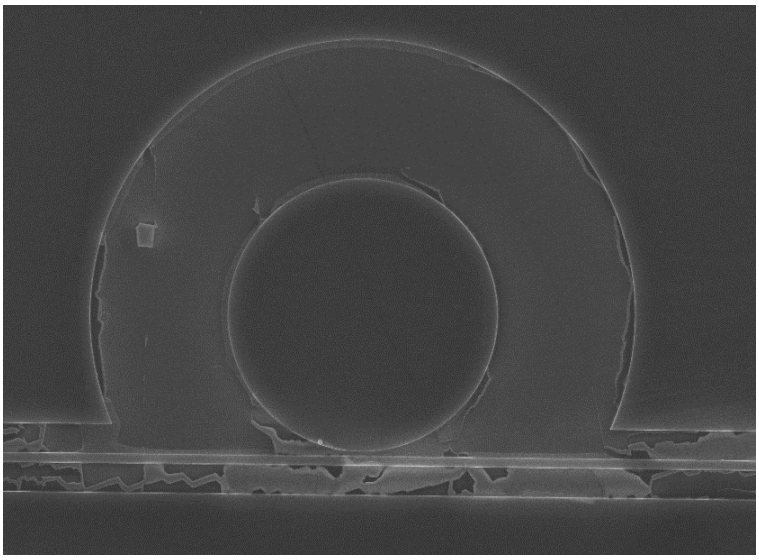

Figure 57 - Top view SEM image of the bottom-layer-graphene transferred on a SiN microdisk resonator.

As we can see from the SEM image, the graphene layer completely covers the microdisk and is almost a perfect intact film on top of it. However, as it meets the 400 nm height difference around the periphery of the resonator it cannot withstand the tension caused by this height difference and starts to tear. Fortunately, most of these tears do not cause major issues in the performance of the optical devices, as we mainly need graphene to cover (and be attached to) the microresonator. I actually need to remove the graphene from other parts of the structure including the access waveguides in the following steps. Therefore, as long as the transferred graphene covers the top of the microresonator, the transfer process is considered successful.

Figure 58 shows the result of Raman spectroscopy on the transferred film. The G band appears at approximately 1583 cm^{-1}, and the 2D band is located at approximately 2680 cm^{-1}. The 2D band can be used to determine the number of layers of graphene. This is because in the multi-layer graphene, the shape of 2D band is different from that in the single-layer graphene. As shown in Figure 57, the higher intensity of 2D band as compared to G band proves that the transferred layer of graphene is a high quality single-layer film.

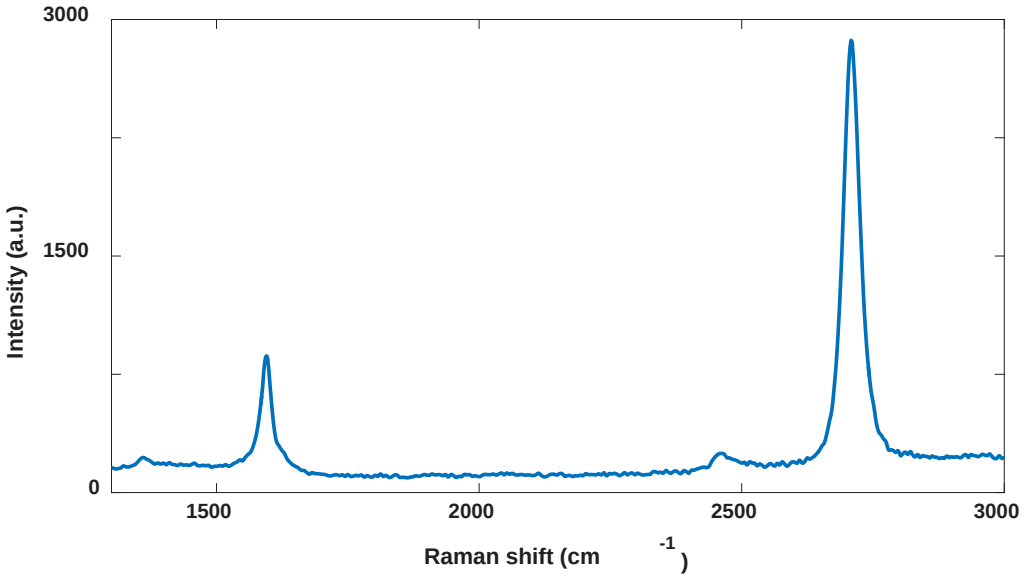

Figure 58 - Raman shift of the transferred graphene.

5.2.4 Patterning the Bottom-layer Graphene Over the Optical Devices

After successful transfer of the bottom-layer-graphene on the passive SiN devices, I need to pattern and remove graphene from unwanted areas, both to minimize optical loss caused by graphene and also to avoid short circuiting the bottom and top plates of the capacitor to be formed on the devices. I use the combination of EBL and dry-etching using O_2 plasma to pattern the graphene. The e-beam resist that I use should have some properties

including, being easily removable from the substrate after the EBL/etching process without causing tears/damages to the graphene layer. The resist's corresponding solvent should also be compatible with the SiN/SiO_2 substrate so that it does not damage/etch the passive structures already fabricated on the substrate. This is why I selected PMMA as the e-beam resist to pattern graphene. PMMA is the same polymer that was previously used in the graphene transfer process, so there is no compatibility concerns. Therefore, if processed carefully, PMMA does not cause extra damage to the graphene layer.

After successful transfer of graphene on the chip, the patterning step is as follows. I first spin coat A6 PMMA from Microchem on the chip at 3000 rpm (speed ramp of 1500) for 60 seconds. Then bake it at 180º C to remove the excess solvent for 90 seconds. After baking I spin coat ESPACER 300Z at 2500 rpm (ramp speed of 2500) for 30 seconds on the sample to help avoid charge-up issues. I then load the chip in the EBL system and write the desired pattern on the sample. It should be noted that PMMA is a positive-tone e-beam resist meaning that the exposed areas will dissolve in the developer and the unexposed areas remain on the chip. So, In order to remove graphene from the undesired areas on the chip (e.g., access waveguides and the bottom of the trenches around the devices) and also pattern the graphene layer as the bottom plate of the capacitor on top of the photonic structures, I should expose these areas to the e-beam. After the EBL process, I develop the sample in a 1:1 solution of MIBK:IPA for 2 minutes to remove PMMA from the e-beam exposed areas. Now that PMMA is patterned on the sample, I use a mild O_2 plasma in an RIE system to etch/burn away graphene from the exposed areas on the sample. PMMA is easily removed in O_2 plasma, so the power and the duration of the O_2 plasma has to be short enough not to consume the whole PMMA film that is protecting the parts of the

sample. After the O_2 RIE etching process, I remove the PMMA (resist) from the unexposed areas using Acetone. Here again I use Acetone vapor instead of immersing the sample in Acetone bath to avoid damaging the graphene in the liquid. Vapor Acetone dries out without leaving any residues on the sample, and there is no need to use N_2 blow gun to facilitate the drying, as it may cause damage to the graphene layer. Figure 59 shows a top view SEM image of the bottom-layer-graphene (i.e. bottom capacitor plate) on a SiN microdisk resonator after being patterned using PMMA. As we can see, the graphene is successfully removed from the access waveguide, the bottom of the trenches around the microdisk resonator, and some parts of the microdisk resonator without being torn or damaged where it is supposed to stay.

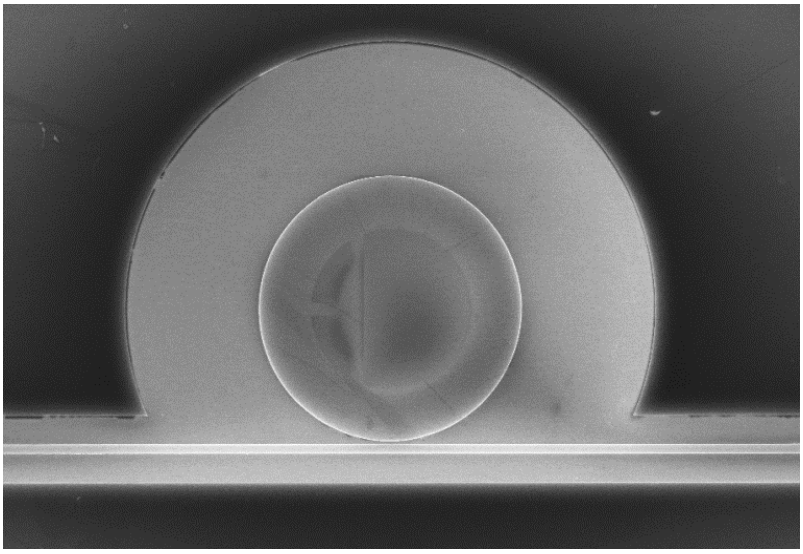

Figure 59 - Top view SEM image of the bottom-layer-graphene on a SiN microdisk resonator after being patterned using EBL and dry etching in O_2 plasma.

5.2.5 Making Metal Contact to the Bottom-layer Graphene

After successfully removing graphene from unwanted areas and patterning the graphene layer on top of the passive SiN devices, I proceed to add the metal contact on the

bottom-layer graphene to serve as the contact to the bottom plate of the capacitor. The contact should be placed away from the outer-radius, either well inside the resonator or outside of it. The reason behind this is that, as seen in Figure 60, the optical field of the fundamental TE mode (i.e., electric field in the place of the resonator) in a typical microdisk resonator resides close to the periphery (i.e., outer-radius) of the microdisk. Due to the high optical loss of metals, placing the metallic contact where the optical field is strong (i.e., close to the outer-radius) considerably reduces the Q of the microresonator.

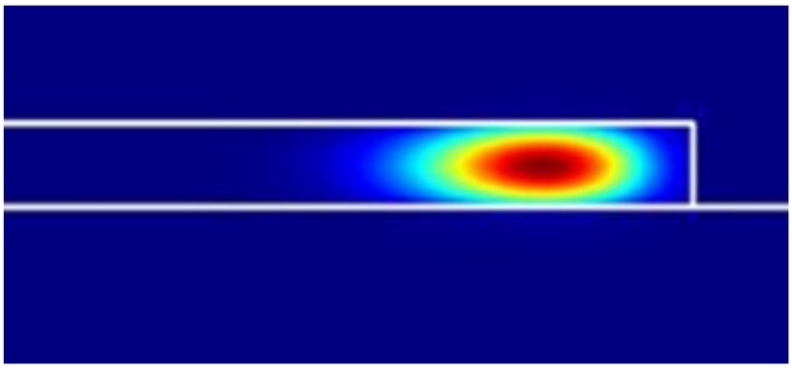

Figure 60 - Cross-sectional profile of the Poynting vector for the fundamental TE mode in a typical microdisk resonator.

In addition to the optical loss, I need to consider the contact resistance of the metallic contact to graphene. This seriously affects the modulation speed. Other than the location and the shape of the contact, the choice of metal is an important factor in achieving low contact resistance with graphene. Using all these criteria, I optimized the location, the shape, and the material of the metallic contact to the bottom-layer graphene.

Here I use Ti/Pd/Au 1.5/45/15 nm as the contact to graphene. I use the combination of EBL, e-beam metal evaporation, and lift-off to form the Ti/Pd/Au contact to the bottom-layer graphene. I again use PMMA as the e-beam resist for the lift-off process due to its

compatibility with graphene. I first spin coat A6 PMMA from Microchem on the chip at 3000 rpm (ramp speed of 1500) for 60 seconds. Then bake it at 180º C to remove the excess solvent for 90 seconds. After baking I spin coat ESPACER 300Z at 2500 rpm (with ramp speed of 2500) for 30 seconds on the sample to help avoid charge-up issues. I then load the chip in the EBL system and write my desired pattern on the sample. After the EBL process, I develop the sample in a 1:1 solution of MIBK:IPA for two minutes to remove PMMA from the e-beam exposed areas. Now that PMMA is patterned on the sample I load the sample in an e-beam metal evaporator and pump down the chamber to the low 10e-6 Torr range before evaporating 1.5 nm Ti, 45 nm Pd, and 15 nm Au, successively. After the evaporation process, I perform the metal lift-off process as follows. I leave the sample in Acetone for two hours. Then, after most of the large metal pieces have been removed from the sample, I place it in a second (fresh) container of Acetone. This helps to keep floating metal pieces from redepositing onto the sample. I keep the sample immersed in Acetone for another 30 minutes. In the next step, I place the sample in IPA and change the IPA solution a couple of times to completely remove any Acetone left in the solution. I then take the sample out of the IPA solution and leave it to dry by itself under a fume hood. Figure 61 shows a top view SEM image of the bottom-layer graphene on a SiN microresonator with metal contact. As we can see from the figure, the contact is well inside the microdisk and completely away from its periphery (where the optical modes reside). At this stage the bottom plate of the capacitor is completely formed, and I move on to the next step, i.e., depositing the capacitor dielectric before transferring the second (top-layer) graphene.

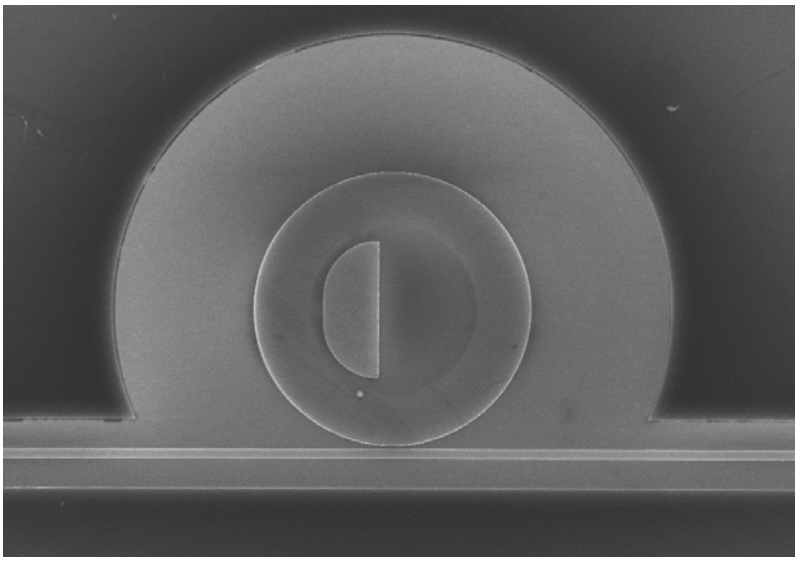

Figure 61 - Top view SEM image of the bottom-layer-graphene on a SiN microdisk resonator with metal contact made to the bottom-layer-graphene.

5.2.6 Depositing Alumina on Graphene

The material I choose as the capacitor dielectric is alumina (Al_2O_3). It is a high-k dielectric material which enables higher charge accumulation in the (graphene) capacitor plates (i.e., more shift in the resonance of the devices). Alumina can be deposited via atomic layer deposition (ALD), which produces conformal, pinhole-free films with atomic level control over the thickness of the film. ALD films are grown on a substrate by exposing its surface to alternate gaseous precursors. For the case of alumina deposition, I use Trimethylaluminum (TMA) and water as the alternating precursors at 250º C.

Unfortunately, ALD of alumina (or other thin films for that matter) on pristine graphene is not trivial, because there are no dangling bonds on the untreated graphene surface, which are needed for chemical reactions with the ALD precursors. As shown in Figure 62, performing 90 ALD cycles of alumina on pristine graphene results in

disconnected islands of alumina instead of a uniform film. The alumina film has in fact preferentially formed on graphene edges and defect sites.

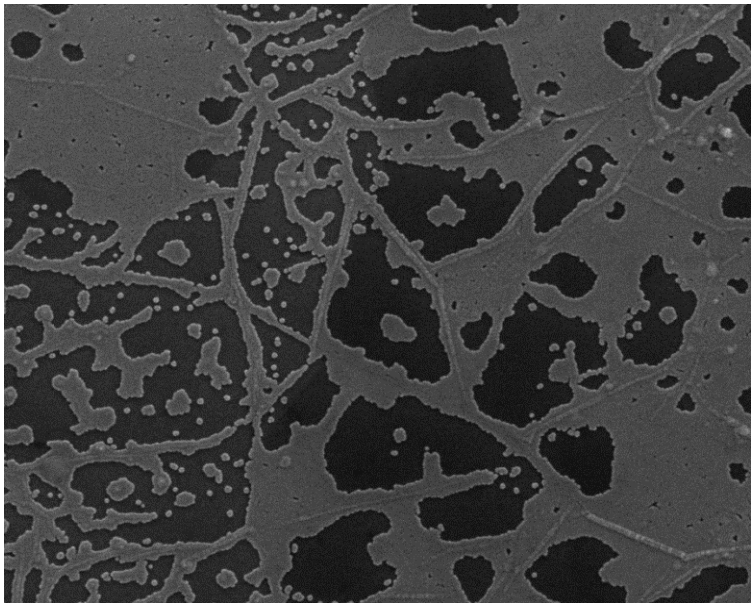

Figure 62 - Top view SEM image of a graphene layer after 90 cycles of alumina ALD performed on it without any pretreatment.

The solution to improve the uniformity of the ALD of alumina on graphene is to evaporate a very thin seed layer (~1 nm) of Aluminum (Al) on pristine graphene before performing ALD on it. The Al seed layer will oxidize before the ALD process starts and becomes alumina, which will help increase the uniformity of the final film (alumina seed layer plus the ALD alumina). Figure 63 shows the SEM image of the sample formed by 90 ALD cycles of alumina on graphene after functionalizing the graphene layer with ~1 nm Al as the seed layer. The dramatic improvement in the quality of the deposited alumina as compared to the case of the ALD growth with no seed layer (Figure 62) is evident from Figure 63.

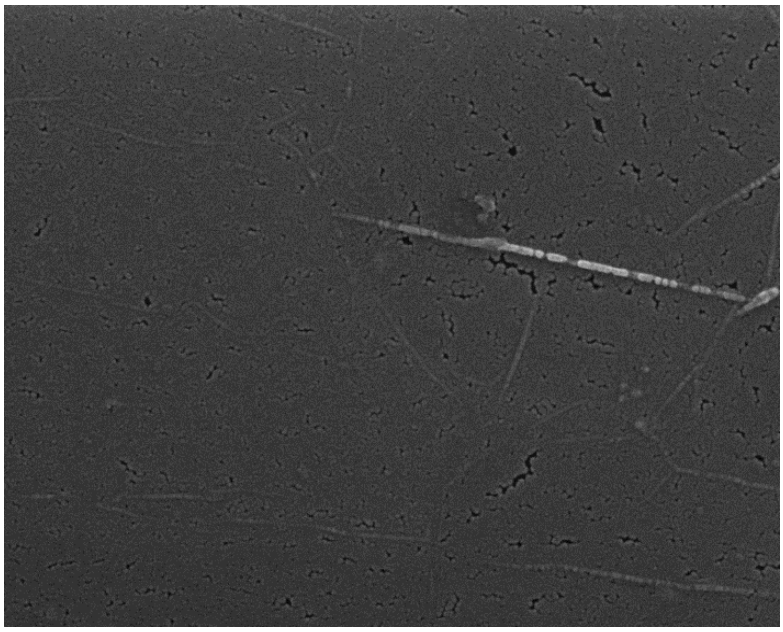

Figure 63 - Top view SEM image of a graphene layer after 90 cycles of alumina ALD performed on it (with a ~1 nm Aluminum seed layer).

So, back to the fabrication steps of the graphene-SiN sample. After successful metallization and lift-off on the bottom-layer graphene, the graphene-coated sample is placed inside the metal evaporator chamber. The chamber is then pumped down to the low 10e-6 Torr range, and then 1 nm Al is evaporated on it at the rate of 0.1 Angstroms per second. The final thickness is confirmed with ellipsometry measurement. The sample is then taken to the ALD chamber, and about 14 nm of alumina is coated on it via alternating pulses of water and TMA. Figure 64(a) and Figure 64(b) (higher magnification) show the SEM images of the sample after alumina deposition. The final result is a uniform pinhole-free alumina film grown on bottom-layer graphene (this is evident from Figure 64(b)).

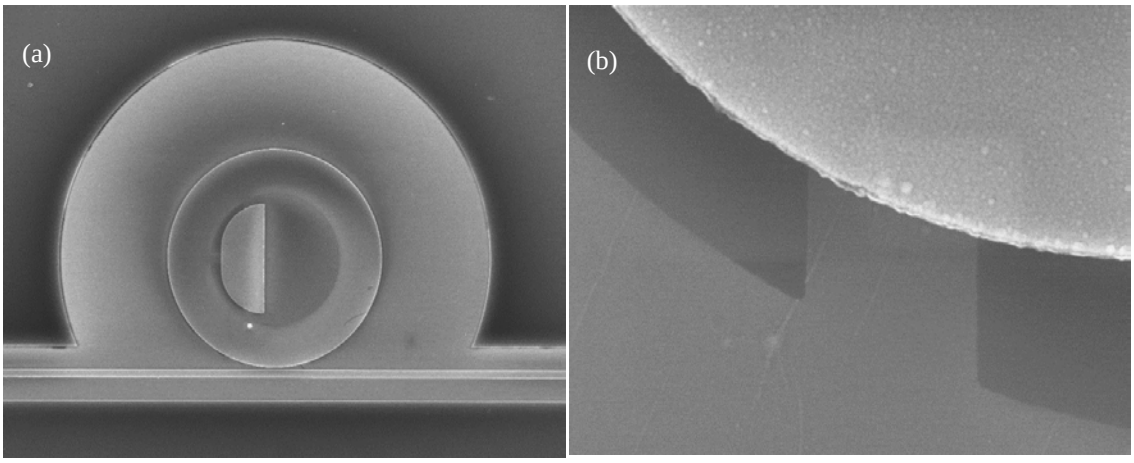

Figure 64 - (a) Top view SEM image of the bottom-layer graphene on a SiN microdisk resonator after ALD of Alumina; (b) same as (a) at higher magnification.

5.2.7 Transfer of Top-layer Graphene on Optical Devices

After successful deposition of the dielectric material, I proceed to transfer the second layer of graphene (top-layer graphene) on top of the alumina layer using the process described earlier. This graphene layer will serve as the top plate of the capacitor on top of the device. Figure 65 shows the top-view SEM image of the top-layer graphene layer transferred on the alumina layer. As we can see in the figure, the top graphene layer completely covers the microresonator area and is almost a perfect intact film on top of it. As discussed earlier, the tears on the graphene at the periphery of the microdisk resonator do not cause any problems; and the transfer process is considered successful as long as the transferred graphene remains a high-quality layer on top of the optical devices.

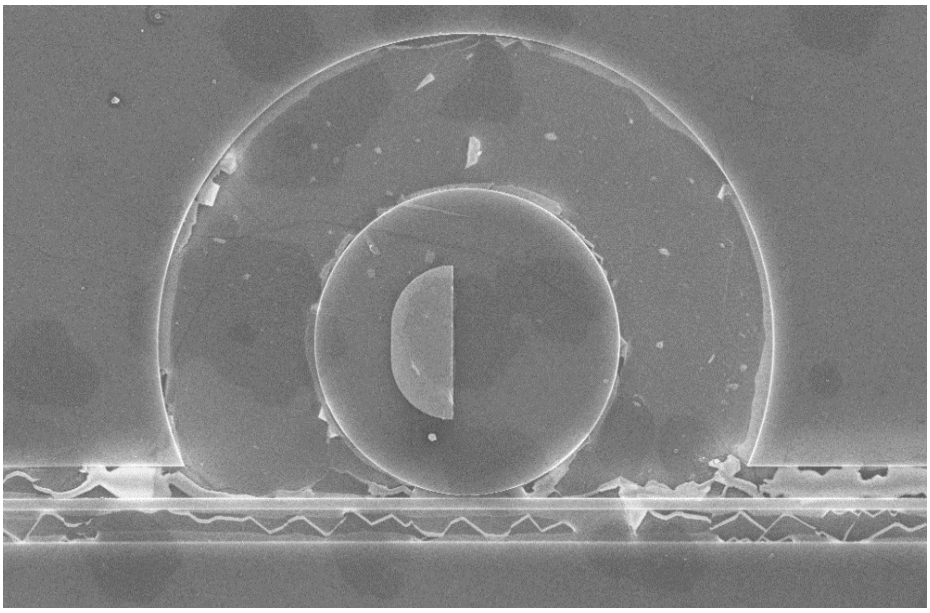

Figure 65 - Top view SEM image of the top-layer-graphene transferred on a SiN microdisk resonator.

5.2.8 Patterning the Top-layer Graphene Over the Optical Devices

After successful transfer of the top-layer graphene, I need to pattern and remove graphene from unwanted areas using a similar process composed of EBL and O_2 dry-etching as explained for case of the bottom-layer graphene. After the RIE etching process, I remove the PMMA from the unexposed areas using vapor Acetone. Figure 66 shows the top-view SEM image of the top-layer graphene (i.e., the top capacitor plate) on a SiN microresonator after being patterned using PMMA. Figure 66 clearly shows that graphene is successfully removed from the access waveguide, the bottom of the trench around the microdisk resonator, and some inner parts of the microresonator.

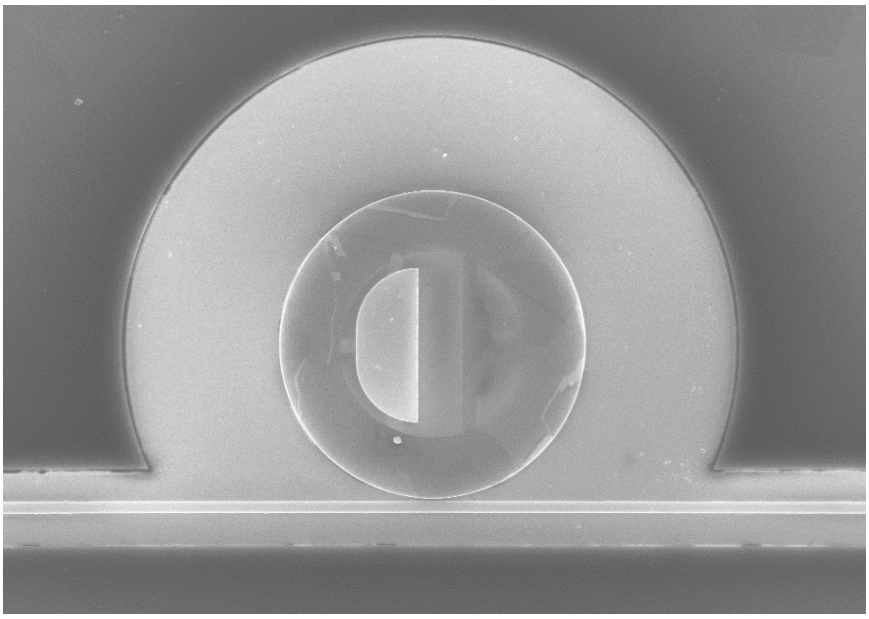

Figure 66 - Top view SEM image of the top-layer-graphene on a SiN microdisk resonator after being patterned using PMMA and O_2 plasma.

5.2.9 Making Metal Contact to the Top-layer Graphene

To complete the fabrication of the double-layer capacitive graphene structure, I must add the metal contact to the top-layer graphene. Here I use a similar process to the one in case of the bottom-layer graphene (i.e., using the combination of EBL, e-beam metal evaporation, and lift-off) to form the Ti/Pd/Au contact to the top-layer graphene. Figure 67 shows the top-view SEM image of the top-layer graphene on the SiN microdisk resonator with the Ti/Pd/Au metal contact. At this stage, the capacitor is completely formed.

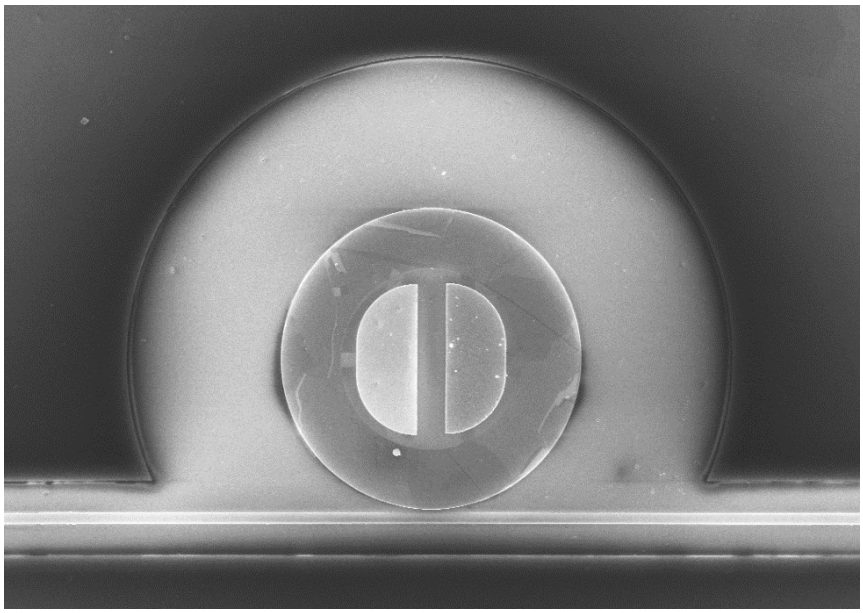

Figure 67 - Top view SEM image of the top-layer-graphene on a SiN microdisk resonator with metal contact made to the top-layer-graphene.

5.2.10 Depositing Protective Alumina Layer on Top of Top-layer Graphene

The final fabrication step after forming the double-layer graphene capacitor on top of the SiN microdisk resonator is to deposit another layer of ALD alumina to protect the top-layer graphene from the next fabrication steps on the device. Similar to the case of ALD deposition on the bottom-layer graphene, I first grow a ~1 nm Al seed layer before growing ~14 nm alumina in an ALD chamber. Figure 68 shows the SEM of the sample after top alumina deposition with different magnifications. It is clear from Figure 68 that the final result of my process is a uniform pinhole-free alumina film grown on the top-layer graphene.

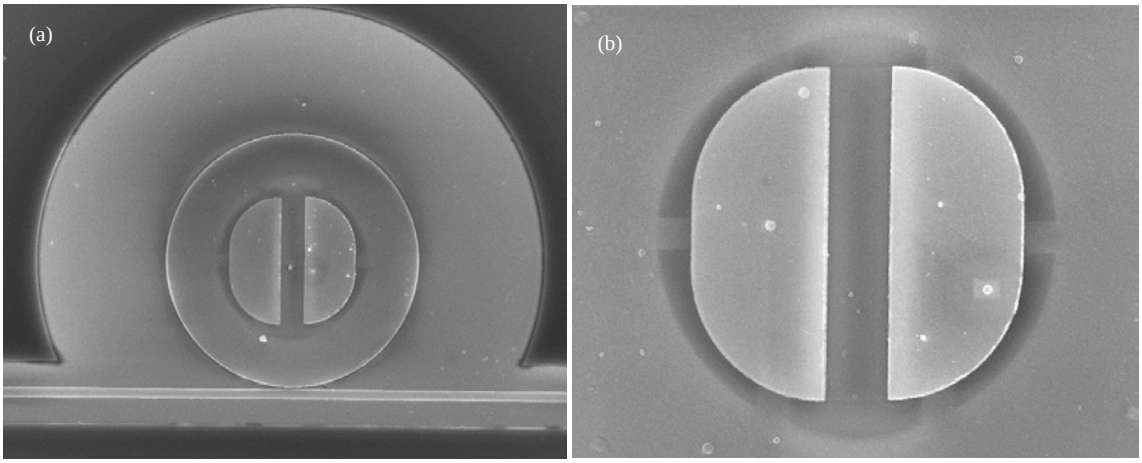

Figure 68 - (a) Top view SEM image of the bottom-layer graphene on a SiN microdisk resonator after ALD of alumina; (b) same as (a) at higher magnification

5.2.11 Growing Buffer Oxide on the SiN Devices

Up to now, I showed different steps required to fabricate a double-layer SiN graphene modulator all the way from growing high quality SiN film in a low-pressure chemical vapor deposition (LPCVD) chamber on oxide wafers to transferring two layers of graphene and patterning them and depositing low-resistance metal contacts. After these steps, major fabrication steps of the modulator are basically complete. However, limitations in characterization equipment force me to add one final step. The contacts that are made in the middle of the microresonators are only 2-3 μm in size and only 2-3 μm apart. On the other hand, standard characterization probes are much larger than these contacts. Thus, I need to form much larger pads (on the order of 100 μm by 100 μm) on these smaller contacts to be able to electrically characterize the device. On the other hand, as discussed previously, the high optical absorption coefficient (or optical loss) of metals prevents me to use large pads directly on top of the microresonators (on the same surface as the microresonators). This is why I have to deposit around 2 μm of buffer insulator

(PECVD SiO_2) on top of the chip, then, make via openings on top of the contacts by etching back the insulator, and filling the vias up with metals to form the necessary large pads on top of the device for characterization purposes. Figure 51 shows the schematic of the final device.

Unfortunately, as shown in Figure 69(a) and Figure 69(b), after depositing the 2 µm buffer oxide on top of the chip, poor adhesion of graphene to the substrate in the periphery of the optical devices, and the stress of the thick buffer oxide film caused the buffer oxide to delaminate from the bulk of the chip. However, the oxide directly on top of devices is intact. This has caused a 2 µm bump of oxide on the devices with no oxide covering the rest of the chip. The areas with darker green color are the areas where the buffer oxide is not delaminated. Due to this 2 µm height difference no further processing (e.g., e-beam resists spin coating and e-beam lithography) can be done on this chip. So, basically, this fabrication approach failed; therefore I tried other approaches.

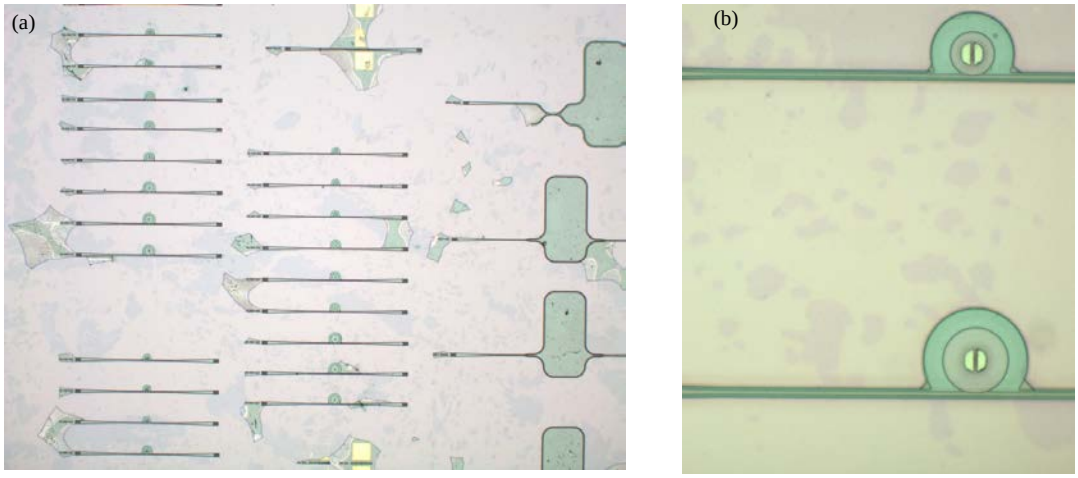

Figure 69 - Optical image of the chip after the buffer oxide delamination from the top of it at (a) low magnification, and (b) high magnification.

So, how to avoid sample failure for the next round? I need graphene only on top of the resonators and some of the waveguides, i.e., an area a few percent of the whole area of the chip. So a question might be raised why I kept this much graphene in the unwanted areas on the chip in the first place. Well, to answer this I should first review the process that I use to pattern and remove graphene from unwanted areas. As discussed previously, I work with PMMA to pattern the graphene and etch it away using O_2 plasma. Since PMMA is a positive-tone resist, areas of graphene that are supposed to be etched away need to be directly exposed with e-beam. So, if I want to remove graphene from all over the chip except on the active regions, it would take very long which is not reasonable. This is why I had chosen to only remove graphene from the areas that had to be removed and left the rest untouched. So why not use a negative-tone resist so that only the wanted areas are exposed, and basically reduce the exposed area to a few percentage of the chip size? Unfortunately, neither of the conventional negative tone e-beam resists are compatible with my structure. HSQ (negative-tone e-beam resist) needs BOE wet etching after O_2 etching process to remove its residues, and BOE will damage the substrate of the chip. On the other hand, for the case of Ma-N (another negative-tone e-beam resist), my experiments showed that graphene tends to stick to Ma-N better than to the substrate which causes poor adhesion to the surface of the chip after removing Ma-N. Since, changing the e-beam resist did not seem to be a viable option, I devised three other approaches to get around the buffer oxide delamination issue. I explain these approaches in the next sections. One of the approaches is based on removing the unwanted graphene using PMMA exposed with Deep UV or higher e-beam currents. The second one is based on wafer bonding approach. The third one

is based on planarizing the chip after etching SiN devices to avoid having to deposit thick PECVD buffer oxide followed by making via openings.

5.3 Other Fabrication Trials

5.3.1 Exposing PMMA with Deep UV or Higher E-beam Current

Well, as I discussed in the previous section, it was basically the unwanted graphene in the periphery of the devices that caused the failure. If we remember, the buffer oxide directly on top of the optical devices (where the graphene was partially etched) did not delaminate. This suggests that if we etch some lines in the graphene layer on the periphery of the devices, the buffer oxide will have several direct connections to the bottom substrate whereby increasing its adhesion, to hopefully resist delamination from the chip. This will only add a few more percent of writable area and only incrementally increase the e-beam exposure time. Figure 70(a) shows the AutoCAD drawing of some part of the pattern that will be used to expose the new sample. The red areas are critical areas on top of the active devices. The white lines are the new added patterns that are supposed to make openings in the unwanted areas of graphene so that the buffer oxide (that will be deposited in the following steps) will have direct contact to the substrate to improve its adhesion. Well, a new SiN chip was etched, the bottom-layer graphene was transferred and exposed using the new pattern (with the adhesion promoting lines added), followed by O_2 plasma etching. The bottom-layer contacts were lifted-off. Then, the dielectric layer was deposited using the combination of Al seed layer evaporation and alumina deposition in an ALD chamber. Then, the top-layer graphene was transferred and exposed using the new pattern (with the adhesion promoting lines added), followed by O_2 plasma etching. The top-layer contacts

were then lifted-off. Then, the protective alumina layer was deposited using the combination of Al seed layer evaporation and alumina deposition in an ALD chamber. Then, 2 µm PECVD buffer oxide was deposited on the chip. The new etched lines in graphene layers did in fact improve the adhesion of buffer oxide to the substrate, and it did not delaminate during the PECVD deposition step. So, I continued with making via holes in the buffer oxide to access the metal contact in the center of microdisks. Chromium etch mask was deposited on the sample with Ma-N used as the lift-off resist. Unfortunately, after Cr evaporation and when the sample was in Acetone bath to lift-off the exposed parts, the underlying buffer oxide delaminated again (Figure 70(b)). This shows that, although the adhesion of buffer oxide to the substrate had increased due to the new etched lines in graphene layer, the adhesion was still not strong enough.

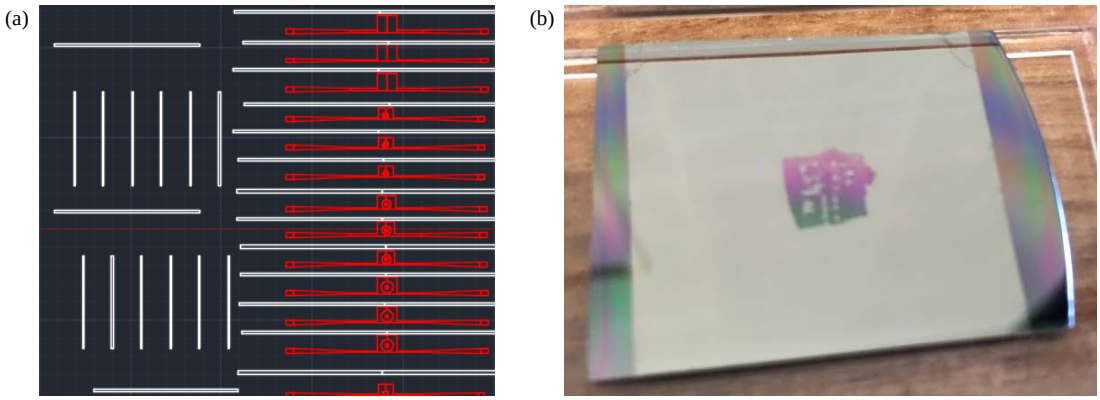

Figure 70 - (a) Snapshot of the new Autocad pattern with added lines to increase adhesion of buffer PECVD oxide. (b) Failed sample after buffer oxide being delaminated from underneath Cr etch mask.

So, I conclude that in order to avoid delamination of buffer oxide from the chip, I need to remove the majority (if not all) of it from the unwanted areas. To fix this issue on the next sample I should try to keep graphene only on the active parts and remove it from unwanted areas. Removing this poorly attached film from bulk of the chip will avoid

delamination of the buffer oxide. As I discussed in the previous section, exposing the PMMA from the whole unwanted area on the chip using PMMA at the standard e-beam current (2 nA) takes very long (on the order of days) which is unreasonable. How about only exposing the critical areas (regions with sub-micron dimension on or around microresonators) at the standard (2 nA) current, then changing the current to 20 nA and exposing the less critical areas (which do not need high resolution exposure). This will considerably reduce the e-beam exposure time from close to four days to only several hours.

But, there is another approach to remove graphene from all over the unwanted areas that takes shorter than high current exposure. Other than e-beam, PMMA is also sensitive to deep ultraviolet (UV) spectrum. So, I can first pattern the critical areas (regions with sub-micron dimension on or around microresonators) using PMMA and e-beam lithography, then, without developing or removing the PMMA re-expose the unwanted areas using deep UV lithography. Finally, develop the doubly-exposed (first e-beam then deep UV) PMMA only once and get rid of PMMA from everywhere except only on active devices. Figure 71 shows the AutoCAD patterns of the etching pattern of one of the resonators. In Figure 71(a) the red areas show the areas that will be exposed with e-beam. Figure 71(b) shows a cropped circle, everything around this cropped circle will be exposed with deep UV, and only the areas inside the cropped circle will be protected. By combining these two patterns for each device I can keep graphene only on the necessary areas and completely remove it from unwanted areas whereby avoiding poor adhesion between buffer oxide and substrate to prevent delamination and failure.

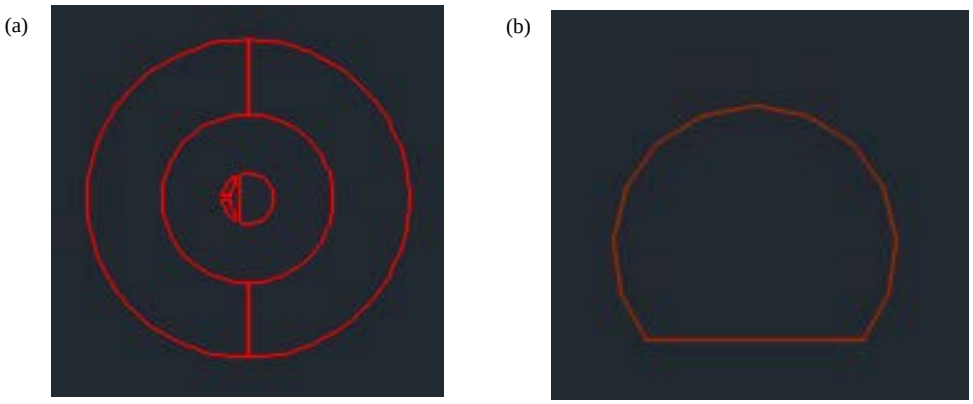

Figure 71 - Snapshot of the Autocad pattern for a microresonator. Part (a) is the pattern that will be exposed in E-beam. Part (b) is the pattern that will be exposed with deep UV lithography.

Before working on this sample I had to optimize the process to expose PMMA with deep UV and develop it afterwards. According to Microchem, PMMA needs dosage of more than 500 mJ/cm^2 in deep UV (248 nm) so that the exposed parts can be dissolved in developer (MIBK:IPA 1:1). However, it was only at dosages above 20000 mJ/cm^2 that I was able to remove the exposed PMMA in developer. This significant difference could be due to the fact that maybe the intensity reader that I use to measure the deep UV intensity is not calibrated, or maybe the optical mask I use is not made with high quality Quartz and in effect has absorption in deep UV. Anyways, I was able to develop and optimize a deep UV process to remove PMMA from the bulk of the sample. The only issue with this process is that after development some few nanometer PMMA residue is left on the sample. However, this is not a big issue for us, as the next step after PMMA development would be O_2 plasma etching of graphene. Basically, the first few seconds of the Oxygen plasma process will get rid of the PMMA residues and then the uncovered graphene will be etched away.

So, with the inclusion of deep UV lithography the process would be modified as follows. After transferring each layer of graphene, I spin coat PMMA on it. I then expose the critical areas (regions with sub-micron dimension on or around microresonators) using e-beam lithography. Then I unload the chip and re-expose the unwanted areas using deep UV lithography, while the areas that were exposed in e-beam lithography are protected/covered using the optical mask. After the second exposure, the chip is developed in MIBK:IPA 1:1 for 2 minutes, followed by O_2 plasma to etch away the uncovered areas.

5.3.2 Inverted Geometry Using Wafer Bonding to Planarize

In the approach that I explain in this section, I will try to use a new device geometry (inverted compared to the initial technique) to avoid having to deposit buffer PECVD oxide and make via openings on it. In this inverted geometry technique, I deposit LPCVD SiN directly on Si (not SiO_2). Then pattern and etch the SiN layer and form optical devices on it. At this stage, the etched devices cannot be optically characterized, because underneath SiN, I have Si which has a higher refractive index than SiN and light will not be confined in the devices fabricated in the SiN film. But there is no need to worry as I will later remove the underlying Si layer and it will only work as a handle/sacrificial layer. As shown in Figure 72(a), the idea is that after etching the optical devices I spin coat flowable oxide (FOx-25) on the wafer and anneal it. Then deposit a couple of microns PECVD oxide on top of it. Then bond an oxide wafer to this wafer. Later on, I will flip the structure and get rid of the Si handle layer. As seen in Figure 72(b), after removing the Si handle layer from the first wafer, the top surface of the wafer is now planarized and there are no more steps that could tear the graphene layers. So, basically, there is no longer any need to deposit PECVD buffer oxide and making via openings on it. Graphene layers can be easily

transferred on the chip and contacts can be made to them. I started making devices using this approach. I deposited 400 nm LPCVD SiN on a Si wafer. Then, etched desired devices on the SiN film. Then I spun FOx-25 on the sample and annealed it, followed by depositing 2 µm PECVD oxide. I then bonded this chip to an oxide wafer using wafer bonding technique. After successful bonding, I flipped the chips and started etching the Si handle wafer using Bosch process. Unfortunately, after the handle layer was thinned down to tens of micron, different layers delaminated from the chip (Figure 72(c)). I believe this sample failed due to the internal built up stress between different layers.

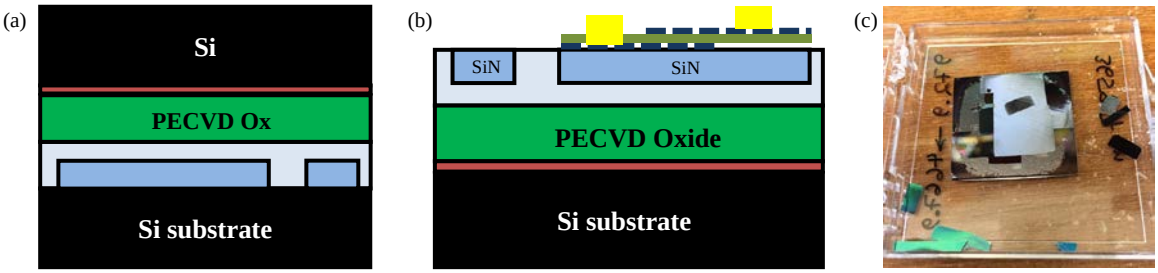

Figure 72 - (a) Schematic showing the concept behind the inverted geometry technique. (b) The final sample after etching the Si handle wafer and transferring graphene and making contacts. (c) Optical image of the bonded chip that failed during back-side etching.

5.4 Final Approach for Fabrication

The final technique that is discussed here is the one that was used for the fabrication of final devices. As shown in Figure 73(a), it is based on avoiding the need for depositing PECVD oxide through planarizing the surface of the chip right after etching the SiN layer using spin-on-glass (here I use FOx-25). By having a planarized surface the graphene layers would be easily transferred onto the surface, and there would be no height difference to cause the graphene layers to tear up at the edges. Therefore, there would not be a need to deposit PECVD buffer oxide and make via openings. However, after spinning a single

layer of FOx-25 the surface does not become perfectly flat and planarized. Figure 73(b) shows the SEM of the cross-section of a SiN on Si sample that has been planarized using FOx-25. As we can see there is still some height variations over the waveguides after being partially planarized with FOx-25. Figure 73(c) which is the result of profilometry on the surface (over the waveguides) also confirms this height difference. Basically, after FOx-25 partial planarization, the 400 nm heigth difference is reduced to less than 100 nm. As will be discussed later, using successive steps of FOx-25 spin-coating and etch back, a perfectly planarized surface was achieved.

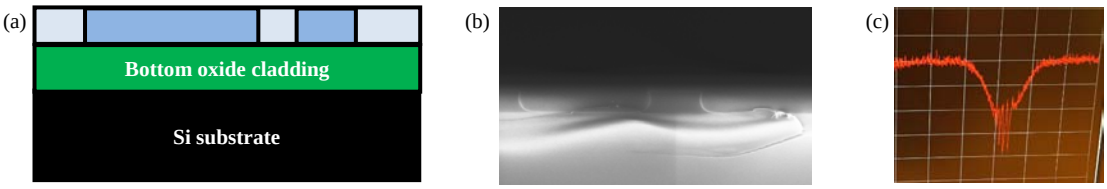

Figure 73 - (a) Schematic showing the devices after being planarized with FOx-25. (b) Cross-sectional SEM images of cleaved facet of SiN on Si waveguides after planarization with FOx-25. (c) Snapshot of the result of profilometry on the surface (over the waveguides).

5.4.1 Fox Planarization

In this section, I will discuss the different steps for fabrication of planarized SiN integrated photonic structures using flowable oxide (FOx-25) to enable transfer of graphene layers without tearing up over the steps of the SiN chip. So, as discussed earlier, the thickness of the SiN film in this work is 400 nm. After etching the SiN layer the step height would be at least 450 nm (with some oxide over-etch included in the SiN etching step). The maximum FOx-25 thickness that I can safely spin coat on the sample is around 1 µm which is achieved at a spin speed of 1000 rpm. The reason behind this is that thicker FOx films tend to crack starting from the edges of the chip (Figure 74(a)), or anywhere

there are particles on the sample which allow for cracks to originate (Figure 74(b)). I tried spinning a second 1 µm thick FOx-25 on the first layer (after it had already been baked on hotplate). It did not help with crack formation, and the final film (after the second spin coating) cracked as well. So, multiple FOx spin coating and etc-back steps are required to achieve a flat surface.

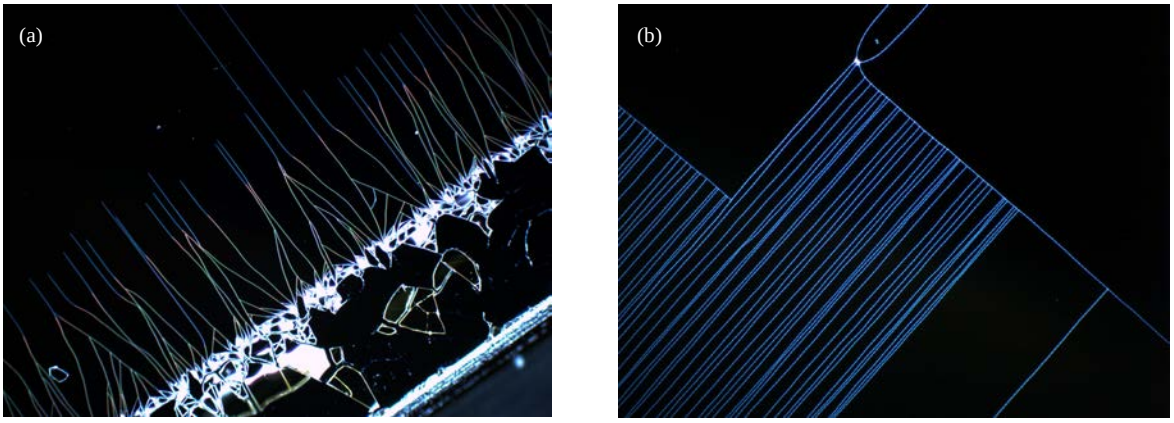

Figure 74 - Dark field optical micrograph of spun FOx with cracks originating from (a) the edges or (b) particles that were on the wafer before spin coating.

So, as discussed earlier, due to the large step height (over 400 nm) on the etched structures, a single step of FOx coating is not enough to completely flatten out the surface, and multiple steps of FOx coating is required. So, every time a 1 µm thick FOx film is spun on the sample, it has to be partially etched back to avoid forming cracks due to excessive stress. In order to protect the passive SiN structures during the etch-back step, he have to protect them with some sort of an etch-stop. Since Fluorine-based plasma is used for the etch-back step, and as discussed in chapter 4, I know that alumina has excellent etch resistance in Fluorine based plasma, I use alumina as my etch-stop. So, I could either fabricate my passive structures in SiN, then cover them with alumina as etch-stop. Or using the alumina hard mask process (the recipe that was discussed in chapter 4) use alumina

itself as the mask for etching SiN structures, then use the alumina residue on top of the structures as etch-stop for the planarization step. As will be discussed later, the second approach was chosen. In the following section, I will discuss the details of making the passive SiN structures.

5.4.1.1 Etching SiN Structures with Alumina as Mask

So, I start with preparing the substrate by growing 4 µm thermal oxide on a prime Si wafer, followed by depositing 400 nm high quality LPCVD stoichiometric SiN on it. Then deposit 50 nm alumina on the wafer using TMA and H_2O as precursors at 250º C in an ALD chamber (Figure 75(a)). About 20 nm of this alumina film will be consumed during etching the SiN passive structures, and the rest will act as etch-stop during the planarization step. Then, 6% HSQ is spun on the wafer at 500 rpm for 60 seconds, and baked at 90º C for 3 minutes. This low spin speed should give around 250 nm of HSQ after baking which is more than enough to etch the 50 nm alumina hard mask. Instead of HSQ I can also use FOx-25 as the e-beam resist and process it under the same EBL conditions as for HSQ. After baking the HSQ, I spin ESPACER 300Z on the sample to help avoid charge-up issues because my substrate (alumina on SiN on SiO_2) is insulating. The sample is then loaded into the EBL system, and is exposed with patterns for passive SiN structures. HSQ is then developed in warm TMAH (40º C) for 30 seconds and rinsed under running DI water for 5 minutes. Patterns on HSQ are then transferred to alumina in a Plasma-Therm ICP system using the recipe which was discussed in chapter 4. The process parameters for etching alumina are as follows: coil power 800 W, platen power 150 W, pressure 5 mTorr, BCl_3 30 sccm, Cl_2 20 sccm. Figure 75(b) shows the schematic of the sample with alumina layer etched using HSQ as mask. The next step would be to use alumina as hard mask and

transfer the patterns to SiN in an Oxford RIE system. The process parameters for etching SiN are as follows: RF power 175 W, pressure 55 mTorr, CHF_3 50 sccm, O_2 5 sccm. Figure 75(c) shows the schematic of the sample with the SiN layer etched using alumina as hard mask. After this etching step around 30 nm of alumina will be left on the sample. Normally, I would remove the alumina hard mask residue from the sample right after etching the SiN layer, however, I keep the alumina residue on this sample because it will serve as etch-stop during the following FOx planarization step.

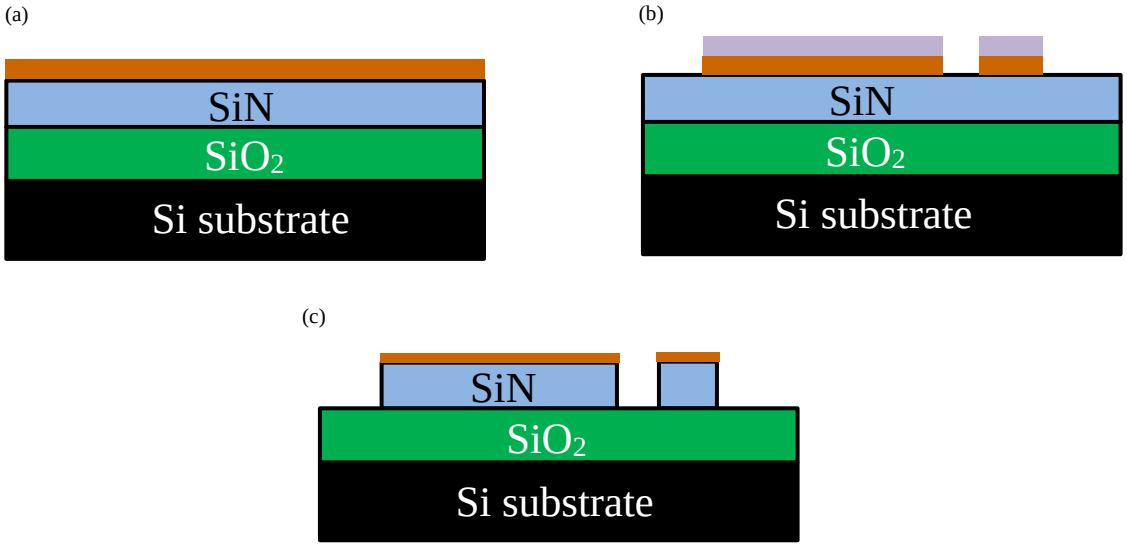

Figure 75 – (a) Schematic of the sample with alumina coated on sample. (b) Schematic of the sample with alumina layer etched using HSQ as mask. (c) Schematic of the sample after the SiN layer is etched using alumina as hard mask.

Figure 76 shows the optical micrograph of the different passive integrated optics structures made on SiN after this step including microring resonators, Mach-Zehnder interferometers, and coupling modulated rings.

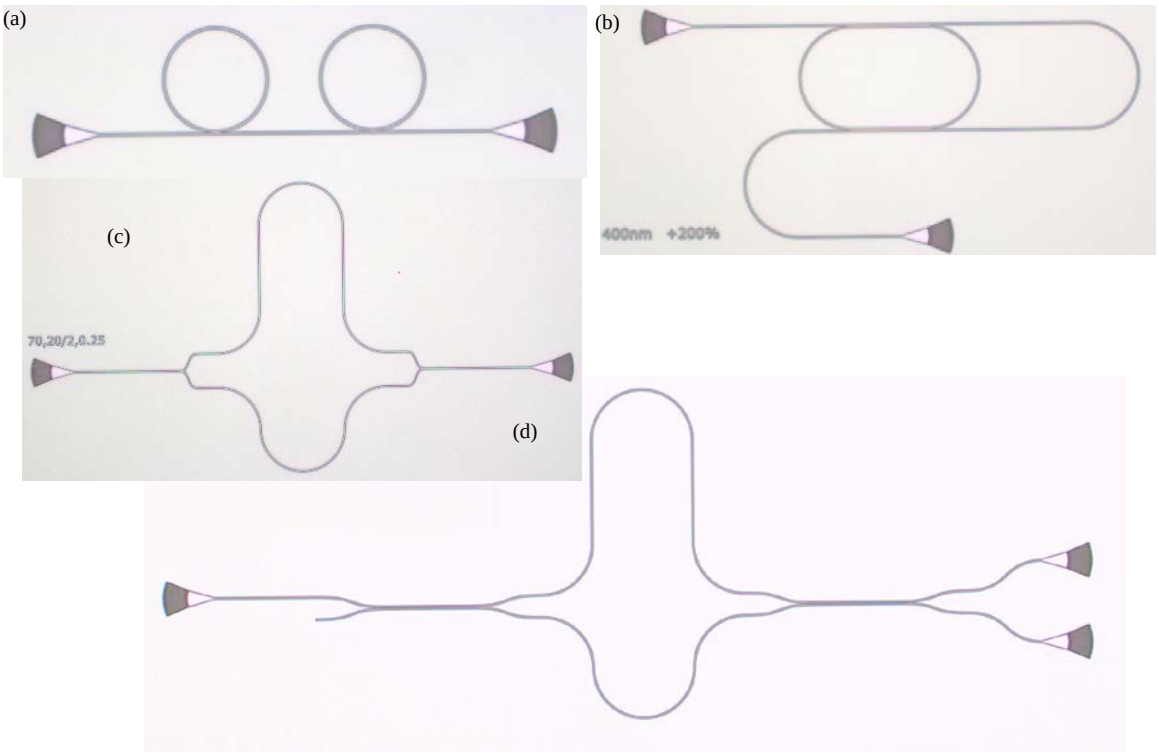

Figure 76 - Different passive SiN integrated optics structures fabricated on the substrate before planarization.

5.4.1.2 Planarizing the Etched SiN Wafer

After successful etching of the passive structures on SiN, I move on to the planarization step. As discussed earlier I use the combination of successive FOx-25 spin coating and etch-back to planarize the sample. I use profilometry to measure the height difference across the sample during different planarization steps.

The first step in the planarization process would be to spin the first FOx-25 layer on the sample. Basically, I spin it at 1000 rpm for 60 seconds then bake it at three different temperatures on hotplate. Starting with 2 minutes at 150º C, followed by 2 minutes at 220º C, and finally 15 minutes at 350º C. Figure 77 shows the result of profilomtery across four waveguides. As we can see from Figure 77(b), the step height after this step is about 50

nm. Although going down from a step height of over 400 nm to 50 nm is a huge improvement, there is still room for improvement through more spin coating steps.

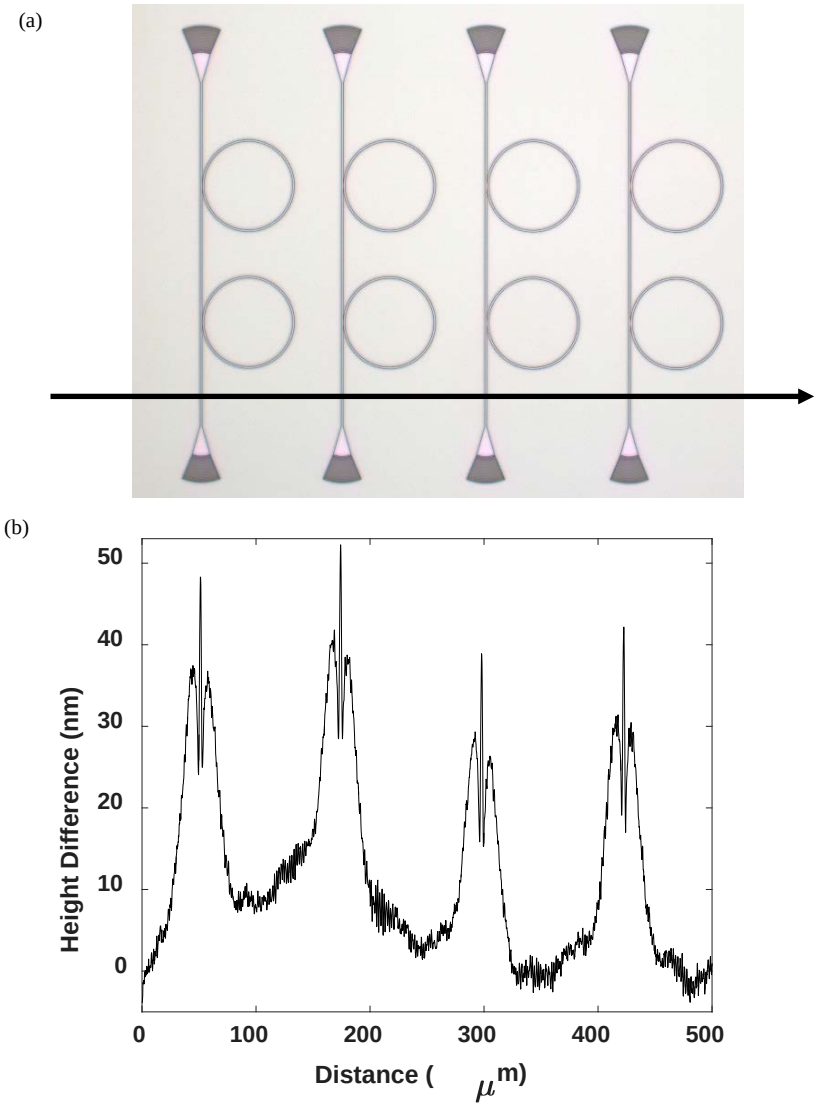

Figure 77 - (a) Micrograph of where on the sample profilometry is performed. (b) Result of the profilometry after spin coating the first layer of FOx.

I cannot spin coat a new FOx-25 layer on the sample at this state. Because, as discussed earlier, cracks will generate on the thicker FOx film. To avoid getting cracks on the sample, I need to etch-back some FOx from the top of the sample before spinning a

new layer. The residue of alumina on the SiN structures will keep them from getting damaged in plasma during the etch-back step. So, I continue to thin down FOx in an Oxford RIE system using an anisotropic oxide etch recipe as follows: RF power 200 W, pressure 33 mTorr, CHF_3 25 sccm, Ar 25 sccm. I etch 400 nm of FOx from the top of the sample. Before spinning a new FOx layer, I deposit ~100 nm of PECVD SiO_2 on the sample to avoid having the second FOx layer directly deposited on top of the previous FOx layer. This will help to avoid crack formation on the sample. I continue to spin coat a new layer of FOx on top of the PECVD oxide using the same parameters as for the first spin process. Figure 78 shows the result of profilomtery across the same waveguides as for the ones in Figure 77(a). As we can see from the figure, the step height after this step is reduced to less than 20 nm. I could continue with coating another layer of FOx-25 to reduce it even more. But, this 20 nm is more than enough to guarantee successful graphene transfer and avoiding graphene tears over the steps across the sample.

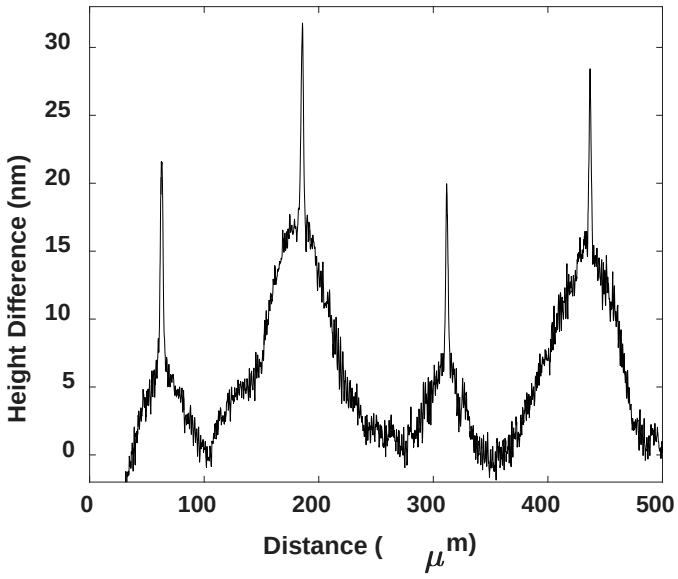

Figure 78 - Result of the profilometry after spin coating the second layer of FOx.

After successful planarization I need to perform a final etch-back to uncover the SiN structures, as I want to have the graphene layers as close to passive SiN devices as possible. The alumina on top of the SiN passive structures will once again serve as etch-stop and help to protect them against plasma damage. So, I etch down FOx in an Oxford RIE system using an anisotropic oxide etch recipe as follows: RF power 200 W, pressure 33 mTorr, CHF_3 25 sccm, Ar 25 sccm. Once the alumina is uncovered I no longer need it, and remove it from the top of my SiN passive structures using a hot Piranha solution. Piranha clean is safe for my sample as none of the layers (SiN, baked FOx) get damaged by going through it. Figure 79 shows the schematic of the final planarized structure after removing the residue of alumina from top of the SiN structures.

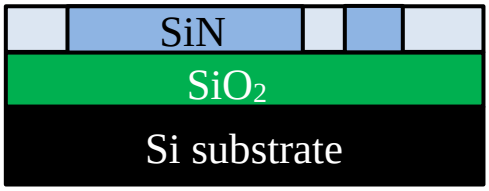

Figure 79 - Schematic of the sample after planarization.

5.4.2 Double-layer Graphene on Planarized SiN

Now that the chip is planarized, I continue with the rest of the fabrication steps, which are as follows: transferring the first layer (bottom-layer) graphene on the sample using CVD grown graphene, patterning the bottom-layer graphene using EBL on PMMA and O_2 plasma, making metal contacts (Ti/Pd/Au) to the bottom-layer graphene using EBL and PMMA followed by metal evaporation and lift-off in Acetone, evaporating the Al seed layer on the bottom-layer graphene, depositing 14 nm ALD alumina as the capacitor dielectric, transferring the second-layer (top-layer) graphene on the sample using CVD

grown graphene, patterning the top-layer graphene using EBL on PMMA and O_2 plasma, making metal contacts (Ti/Pd/Au) to the top-layer graphene using EBL and PMMA followed by metal evaporation and lift-off in Acetone, evaporating the Al seed layer on the top-layer graphene, depositing 9 nm ALD alumina as a final protective layer. Since, all of these steps were discussed in detail in the section 5.2, I will not discuss them here again, and move on to discuss experimental results.

5.5 Experimental Results

Using the fabrication method that was discussed in the last section, double-layer graphene capacitor was integrated with different SiN passive structures. Figure 80 shows optical micrographs of some of the fabricated devices. Figure 80(a) is a SiN microring resonator, Figure 80(b) shows a Mach-Zehnder interferometer, and Figure 80(c) shows a coupling modulated microring resonator. Without the double-layer graphene capacitor integrated with them, they are all just passive structures without any efficient method for tuning or reconfiguration. However, now that a double-layer graphene capacitor is introduced on top of them, we can modify the resonance wavelength or its extinction by applying voltage to the graphene capacitor.

(a) (b) (c)

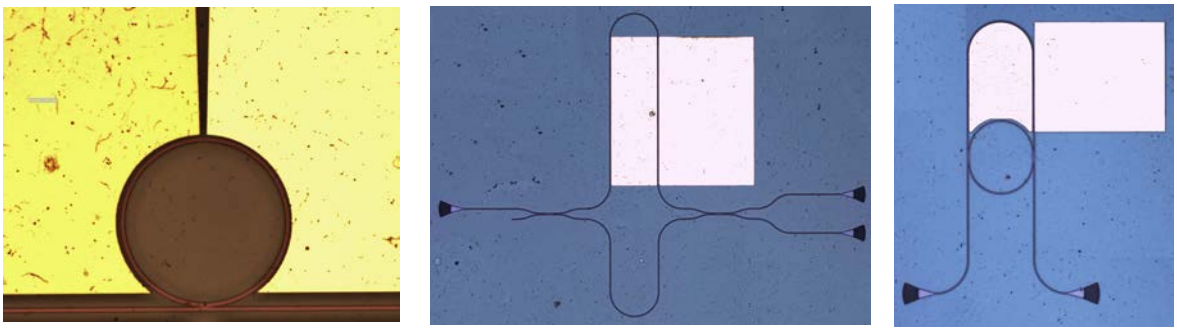

Figure 80 - (a) A microring resonator, (b) a Mach-Zehnder interferometer, and a coupling modulated microring resonator. They are all fabricated on planarized SiN platform with double-layer graphene capacitor integrated with each to add tuning capabilities.

Characterization of the fabricated devices is done using a swept-wavelength transmission characterization setup. A fiber polarization controller is used to adjust the input polarization for the characterization. Grating couplers as shown in Figure 80(b) and Figure 80(c) are used to couple light into and out of the bus waveguides. The output light is detected using a variable gain photo-receiver and sent to a computer through a data acquisition card. Figure 81 shows the TE transmission spectrum of two microring resonators with 20 μm radius coupled to a single bus waveguide. DC voltage is applied only to one of the microring resonators. We can clearly see from Figure 81 that through applying voltage to the graphene capacitor the extinction of only one the resonators is changed while the extinction of the other one stays the same.

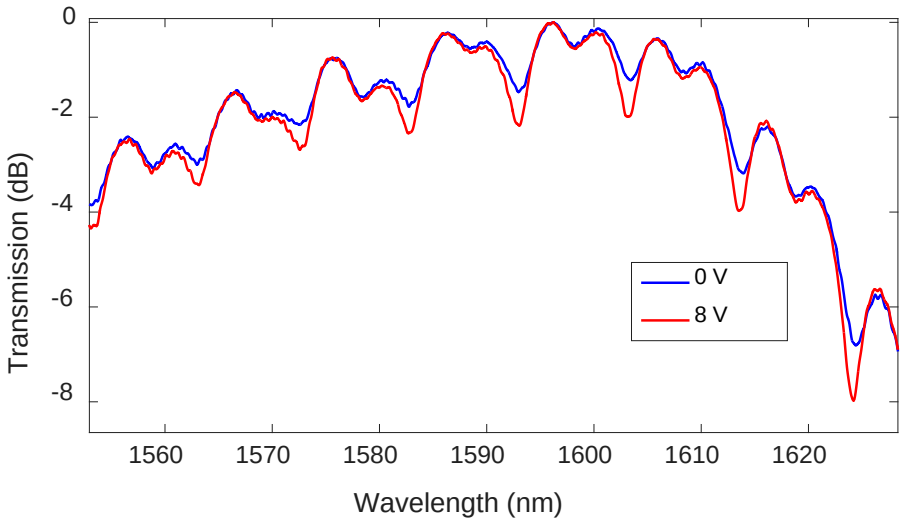

Figure 81 - Transmission spectrum for two 20 µm radius microring resonators for the TE polarization. DC voltage is applied to the graphene capacitor on one of the resonators.

Figure 82 and Figure 83 show one of TE resonances of the same microring resonator. Here we can see that under applying both positive and negative DC voltages the extinction of the microring resonator is modified.

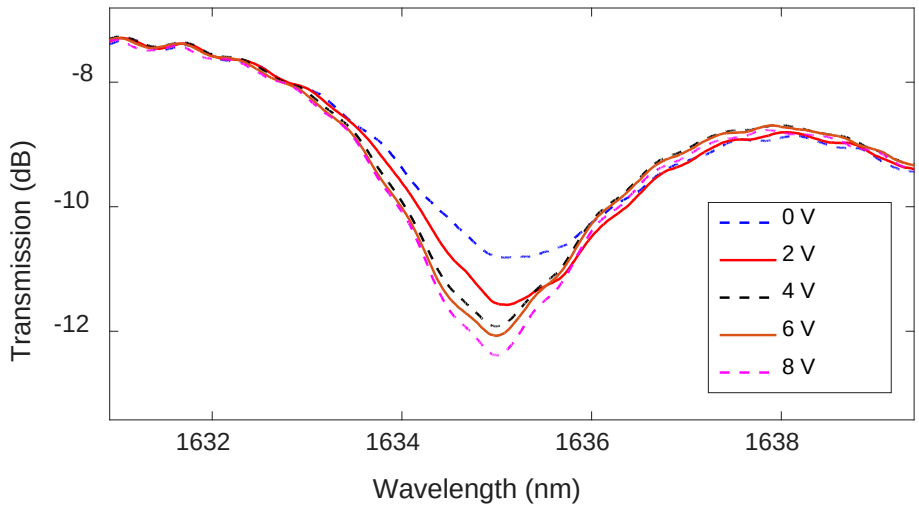

Figure 82 – TE resonance of a 20 µm radius microring resonator under different DC bias conditions from 0 to 8 volts.

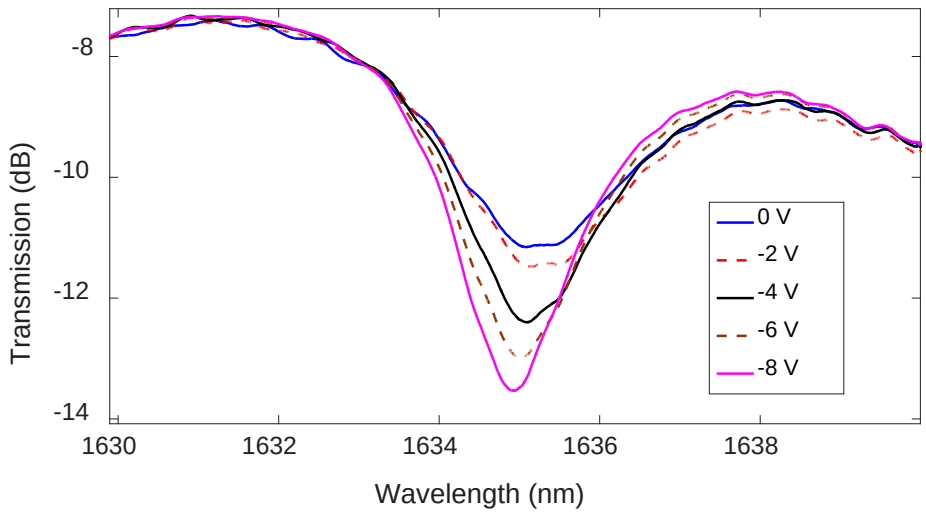

Figure 83 - TE resonance of a 20 µm radius microring resonator under different DC bias conditions from -8 to 0 volts.

In summary, I developed a hybrid SiN-graphene material platform for development of functional devices such as high-speed and low-power modulators. The fabrication process for the hybrid SiN-graphene devices were developed. Through this work, I have developed a reliable process for fabrication of the double-layer graphene on SiN structures and have developed a series of SiN-based hybrid devices with relatively high yield and high performance, and modulation based on the developed device platform was demonstrated.

CHAPTER 6. EPILOGUE

6.1 Summary of Contributions

A double-layer SOI (DLSOI) platform through high-quality bonding of two single-crystalline SOI wafer pieces was demonstrated. The optical quality of the platform was confirmed by achieving high-Q microring resonators with a wide range of radii. For the first time, 2 μm radius ultra-compact microring resonators with intrinsic Q's of 25k in a DLSOI platform for the same microring geometry were demonstrated. At the same time, 20 μm radius multimode microrings for TE and TM polarizations with intrinsic Q's of 350k and 40k, respectively, were achieved. The intrinsic Q of 350k for the TE mode is one order of magnitude higher than that of the best reported result for a similar resonator on a DLSOI platform. Compared to the single-layer Si platform (conventional SOI), the resonators fabricated on the DLSOI platform show similar Q's, which is an indicative of the high quality of the bonding process. This clearly shows that the developed bonding process does not increase the material loss (e.g., due to scattering).

Moreover, cross-polarization in double-layer SOI platform was studied in depth. The unique etched profile of waveguide-coupled microring resonators in DLSOI material platform was theoretically studied. These unique asymmetries introduced during the etching step of devices allow for some quasi-orthogonal modes to be coupled to one another. It was shown that due to these unique asymmetries, fundamental TE and TM modes can be coupled together with only a single step etch. Coupling between the fundamental TM mode of the waveguide to the 9^{th} and 10^{th} TE radial order modes of a microring resonator were experimentally demonstrated. This is the first demonstration of

the coupling of a waveguide mode to such a high order resonator mode with a quasi-orthogonal polarization. An add/drop filter was used to demonstrate polarization rotation from TM to higher radial order TE modes. Overall, the results suggest that the double-layer SOI platform and the unique asymmetries associated with it could be a promising candidate to perform polarization manipulations and rotations.

Moreover, a robust etching process to etch deep profiles in SiN/SiO_2 using alumina as hard mask has been developed and carefully optimized. The etching process has been tested on several devices with promising results. Using the developed etching process, ultra-compact microdisk resonators in SiN with large FSRs were fabricated and shown to have world record high Q's. This is the first time such ultra-small high-Q SiN microresontator are demonstrated. The developed etching process is not limited to the current application. It could potentially be used to etch different materials up to several microns with perfect sidewalls, where conventional e-beam resists such as ZEP, HSQ, and Ma-N do not provide the required etch resistance.

Finally, a hybrid SiN/graphene material platform for development of functional devices such as high-speed and low-power modulators was demonstrated. Surface planarization of etched SiN structures using successive spin coating and etch-back of FOx-25 layers was developed and used for fabrication of active SiN photonic devices. Using the surface planarization technique, a reliable process for fabrication of the double-layer graphene on SiN structures was developed. A series of SiN-based hybrid devices with relatively high yield and high performance and modulation based on the developed device platform were also demonstrated.

6.2 Future Directions

The developed double-layer SOI platform can be used to enable 3-D integration to achieve sophisticated functionalities that are very hard to achieve in single-layer SOI. For instance, microdisk electro-optical modulators can be fabricated in this platform, in which the top and bottom Si layers serve as the capacitor plates (where charge is accumulated), and the resonance wavelength of the device is modulated by carrier dispersion. Alternatively, electro-mechanically tunable photonic microdisk resonators can be realized by partially removing the interface oxide to allow mechanical displacement by applying voltage, which leads to a large resonance wavelength shift. The operating voltage and the power dissipation of these devices will scale with dielectric thickness, which can be pushed to the lowest records using this bonding technique. Therefore, the modulation can be driven at low voltages, and switching will be rather low power and fast with no static power consumption, which can surpass the performance of state-of-the-art modulators based on reverse-biased PN-junction. Furthermore, this material platform can be used to demonstrate functional photonic structures by undercutting the middle SiO_2 layer and filling the gap between the two layers with organic or inorganic materials using polymer infiltration or the atomic layer deposition (ALD) process.

The developed etching process using alumina as hard mask is not limited to just the current application. It can potentially be applied to and used for any application that requires sub-micron feature sizes with deep (over 1 micron) etching profiles. One application would be to etch deep profiles in thick SiN films for dispersion engineering to enable nonlinear effects such as comb generation.

Last but not least, the bandwidth of the operation of SiN-graphene hybrid structures could be increased by reducing the sheet resistance of transferred graphene films through exposing the graphene layers to forming gas to remove any residue of PMMA that might have been left on the surface after the transfer and EBL steps. Another approach to increase the bandwidth would be to reduce the capacitance of the double-layer graphene film through depositing a thicker dielectric. Due to the nature of the wet transfer process, both layers of graphene on the double-layer graphene capacitor are p-doped. Because of this similar doping polarities were only able to achieve small shift in the resonance frequency of modulators through electro-refraction effect. By modifying the doping level of one og the graphene layers and making it n-type (e.g., through immersing the transferred graphene into some wet chemical) much higher shift in resonance and more efficient modulation schemes would be possible.

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